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History and Evolution of CMOS Technology and its Application in Semiconductor Industry

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Abstract

For around five decades, the size of the transistors has been shrinking, and thus the number of transistors in a single microelectronic chip has become possible to increase exponentially. That is, packing density is increasing. The main building block of chip in the semiconductor industry is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). But due to the shrinking of the transistor dimensions, the electrical characteristics of MOSFET are being degraded, which may halt the continuous downscaling of the transistor size. However, various generations of MOSFET have emerged for which we may expect to continue this downscaling for few more years to enhance the computing and communication performance further. Therefore, this article reviews the history and evolution of Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) technology and its application in semiconductor industry and also reviews the recent advances and status of mainstream CMOS as the dominating technology in Very Large Scale Integration (VLSI), current and future trends of RF MOSFETs, and applications of MOSFETs in high power RF electronics for telecommunication sectors. Current researches on advanced MOS and other devices in nano scale regime are discussed also with their structures and various applications. It is hoped that the CMOS will continue to dominate in the semiconductor electronics industry in the few more years to come.

Keywords: Evolution, MOSFET, CMOS, SOI, Technology, Gate Length, ITRS.

I. Introduction

The prime and crucial building unit of the semiconductor electronics industry is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). For the past 50 years, the semiconductor electronics industry has marched at the pace of Moore's Law (ITRS, 2015). Transistor scaling associated with doubling the number of transistors every two years has been and continues to be the unique feature of the semiconductor industry. International Technology Roadmap for Semiconductors (ITRS) revised its projection for the 2016 technology node from 120 nm (ITRS, 1999) to 100 nm (ITRS, 2001, 2002 update), and the targeted gate length for MOSFETs in high-performance logic circuits for 2003 from 85 nm (ITRS, 1999) to 45 nm (ITRS, 2001). Figure 1 shows the evolution of the DRAM capacity and the minimum MOSFET feature size (i.e., the gate length), together with the ITRS targets up to the year 2016.

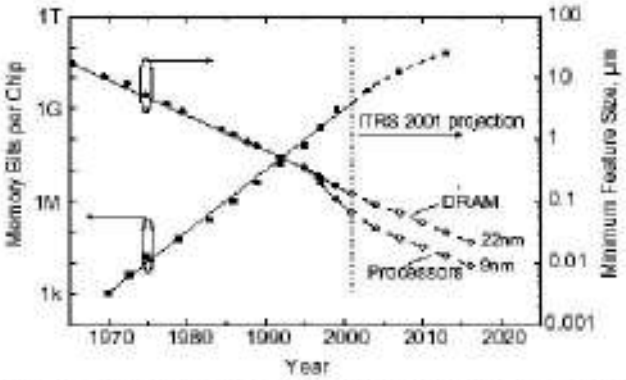

Figure 1: Trends and projections of memory bits per chip and minimum feature size of MOSFETs for DRAM and microprocessors (F. Schwierz *et al.*, 2003)

Figure 2 shows the feature size reduction with time. It is more or less exponential with time. In fact, the current technology allows solid matter to be manipulated at the molecular and atomic level. So, the production and use of nano-scaled systems has become feasible.

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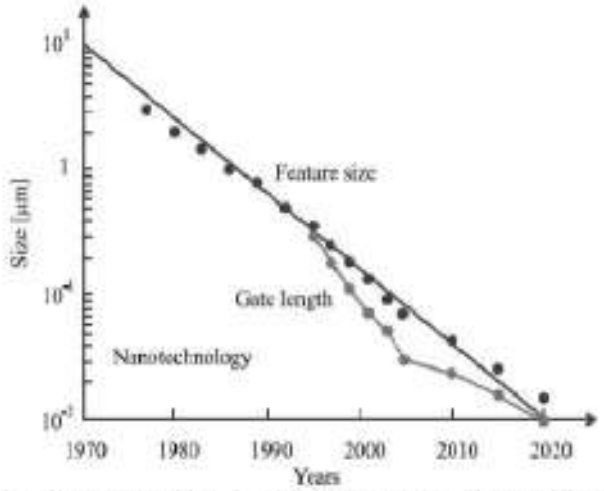

Figure 2: Feature size as a function of time (G. L. Arsov, 2013)

The number of transistors produced per year and the average transistor price with time, as shown in Fig. 3, has been changing exponentially. In 2010, more than a billion transistors were produced for every person living on the Earth. Though scaling is very close to the point to cease since it can't deliver transistor cost reduction further and at 2-3 nm features are only 10 atoms wide at which electrons become uncontrollable.

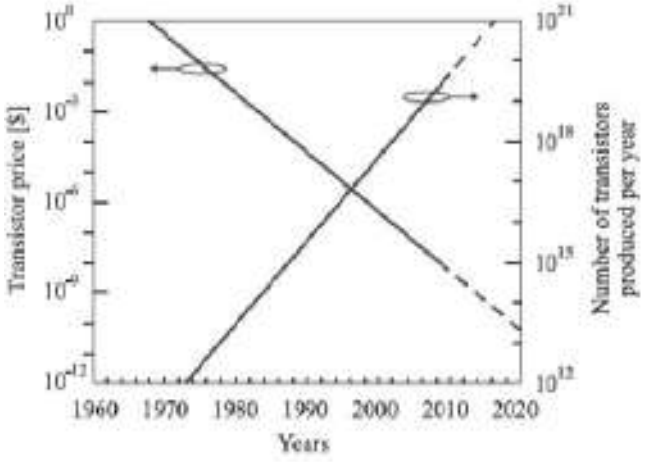

Figure 3: Number of transistors produced per year and transistor price with time (G. L. Arsov, 2013)

Continuous MOSFET scaling and simultaneous increase of chip size led to more and more complex integrated logic circuits with enhanced speed and performance. For example, microprocessors manufactured by Intel Corporation have seen the number of transistors per chip increases from 2300 in 1971 (Intel 4004) to more than 10^8 in 2003, as in Fig. 4. The clock frequency of the processors has been increased from 1 MHz in 1971 (Intel 4004) to about 3 GHz in 2003 (Pentium 4). If processor clock frequency becomes high, it must contain fast transistors that can be achieved by continuous scaling of MOSFETs. Because, transistor speed is inversely proportional to its gate length.

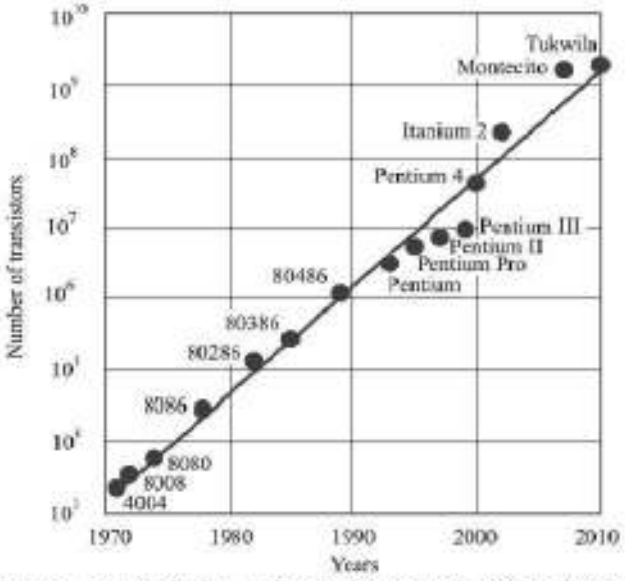

Figure 4: Evolution of transistors per chip of Intel microprocessors (G. L. Arsov, 2013)

In the past, MOSFETs have been considered as 'slow' devices due to various crucial reasons. First, the electron mobility, a measure of how fast the free electrons can move in a semiconductor. In bulk Si mobility (~650 $cm^2/V.s$) is very much lower than in GaAs (~4700 $cm^2/V.s$) and other compound semiconductors. Second, the inversion channel of a MOSFET is formed at the surface of the Si, i.e,, near the Si/SiO_2 interface, thereby subjected to be affected by the interface roughness, crystal imperfections, and interface traps. This causes the mobility degradation of free electrons in the inversion channel (~500 $cm^2/V.s$). But now MOSFETs have been made a faster device by changing its device structure and geometry. Hence it is being still used in the semiconductor industry as a crucial component.

In this review paper, we will discuss about the history, evolution of MOS devices, its various types of structures and its modifications for performance improvement, current and future research trends on MOS devices and then few issues on RF MOS devices. Finally, few application areas of CMOS technology will be mentioned and then concluding remarks on this device will be given.

II. History, Evolution and Research on MOSFET

A. Historical background of MOSFET

Julius Edgar Lilienfeld, a physicist and electronic engineer, is credited with the first patents on the field-effect transistor (FET) (1925). Because of his failure to publish article in learned journals and because high-purity semiconductor materials were not available at that time, his FET patent never achieved fame. But he set out to find a solid-state replacement for the expensive and unreliable thermionic triode that consumed large power and space. Two years later, he presented the idea of the depletion mode MOSFET. He gave the basic concept of controlling the flow of current in a semiconductor (Fig. 5) to make an amplifying device. Metal Oxide Silicon Transistors (MOST), which are built around field-effect principles, dominate semiconductor electronics, today after around 100 years. But the name MOSFET, originated from the Fairchild marketing department in October 1962 (C. H-T. Sah, 1988).

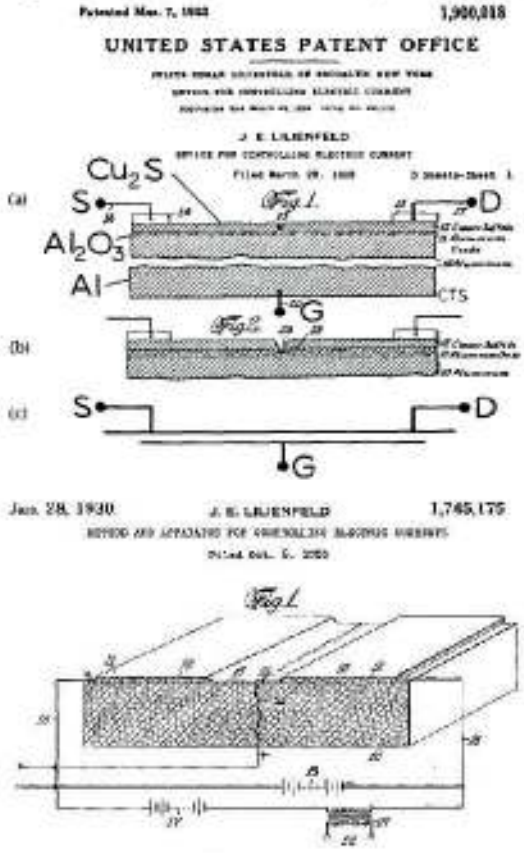

Figure 5: (a), (b) The first two figures in Lilienfeld's 1933 patent (J. E. Lilienfeld, 1933) giving two structures of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) he proposed. (c) The modern circuit symbol of the MOSFET. (d) Current flow control mechan ism in FET (C. H-T. Sah, 1988)

The notion of the inversion-mode MOSFET was proposed by Heil in 1935. After World War II, researchers at Bell Labs were trying unsuccessfully to make field effect devices and apparently they were not aware of the previous work by Lilienfeld and Heil. Ironically, this unsuccessful research on field effect devices led to the birth of the bipolar transistor. Using the ideas of the 'point-contact transistor', Shockley completed the description of the bipolar junction transistor on 23 January 1948 and filed it for a patent on 26 June 1948. Shockley and his two Bell Labs colleagues, Brattain and Bardeen, received the Nobel Prize in Physics in 1956 for the invention of the transistor. Soon the bipolar transistor became the dominating device in semiconductor electronics (C. H-T. Sah, 1988).

The immense delay between the idea and the fabrication of MOSFET was due to the technical difficulties to obtain a good oxide and the lack of fundamental and basic semiconductor notions. In 1956, M. M. Atalla and Dawon Kahng prepared a p-type inversion-channel Si MOSFET using thermally grown oxide for the gate insulator and presented it in 1960 Solid State Device Research Conference, and thus interests in the MOSFET were resuscitated. In 1958, the first integrated circuit was built using two transistors made of germanium using gold wires for interconnections by Jack Kilby at Texas Instruments. Kilby received the Nobel Prize in Physics in 2000 for the 'invention of the integrated circuit'. But the first patent is awarded to Robert Noyce for a monolithic silicon integrated circuit in April 25, 1961. The MOSFET dramatically increased its importance three years later (i.e. in 1963) when Wanlass and Sah of Fairchild Semiconductor first invented the CMOS (Complementary MOS) circuit that reduces power consumption and dissipation with less space due to which MOSFETs have been the most widely used semiconductor device since then. The first two commercial MOSFETs were announced in late 1964, one by Fairchild and a second by Radio Corporation of America (C. H-T. Sah, 1988).

Gordon Moore, a cofounder of both Fairchild and Intel, predicted in 1965 that the number of devices per integrated circuit would increase exponentially with increasing time. This was fitted

on a straight line on a semilog scale graph. This astonishing prediction, which has been named the Moore's Law and is still valid today.

In 1969, Intel develops the first successful PMOS silicon gate transistor technology. These transistors continue to use a traditional silicon dioxide (SiO_2) gate dielectric, but introduce new poly-silicon gate electrodes.

In 1971, Intel launches its first microprocessor named 4004. It was 1/8 inch by 1/16 inch in size, contained 2250 transistors and was manufactured with Intel's 10 pm PMOS technology on a 2 inch wafers. In 1985, Intel386™ microprocessor is released, featuring 275,000 transistors, more than 100 times as many as the original 4004. It was a 32-bit chip and was multitasking, meaning it could run multiple programs at the same time. It was originally manufactured using 1.5 pm CMOS technology. On August 13, 2002, Intel unveils several technology breakthroughs in its forthcoming 90 nm process technology, including higher-performance, lower-power transistors, strained silicon, high-speed copper interconnects and a new low-k dielectric material. This is the first process in the industry to implement strained silicon in production. In 2003, Intel Pentium IV microprocessor was built with 55 million transistors and 512 Mbit DRAM was built with more than half-a-billion transistors.

In January 29, 2007, Intel reveals breakthrough transistor materials, high-k and metal gate that it will use to build the insulating wall and switching gate on the hundreds of millions of microscopic 45 nm transistors inside the next generation Intel® Core™ 2 Duo, Intel Core 2 Quad and Xeon® families of multi-core processors – code named Penryn. Eventually, 53% compound annual growth rate over 45 years has been observed. No other technology has grown so fast for so long period of time. This is mainly driven by miniaturization of transistors that yields smaller in chip size, cheaper in cost, faster in operation and lower in power consumption. This has created manifold revolutionary effects on society and the world economy.

While most integrated circuits fabricated during the 1960s and 1970s were based on bipolar transistors, MOSFET-based circuits gained importance and took over the leading role in the early 1980s. RF electronics technology becomes a part of the semiconductor electronics industry during 1970s and 80s because of its military applications. Then its first civil applications come in 1980s when satellite TV channels started to use GaAs based devices around the 12 GHz frequency band. This created a market economy for the RF electronics. But actual mass volume market economy was created in the early 1990s when cellular telecommunication systems come in to the existence. This market is still growing upward.

B. Chronological development of MOSFET

B.1 Mainstream CMOS

The basic planar bulk structure of MOSFETs as shown in Fig. 6, consisting of a single gate with gate oxide thickness (t_{ox}) of 1.5~3.5 nm, uniformly doped p-type Si semiconducting substrate (frequently called body or bulk) with doping concentration (N_{sub}) 4.5×10^{17} cm^{-3}, and heavily doped source and drain regions (with doping concentration, N_{sd} 9.0×10^{20} cm^{-3}), has not changed much for more than few decades. Only the dimensions and the other features have been reduced continuously to meet the requirements of higher operating frequency or lower propagation delay, lower power consumption and higher packing density.

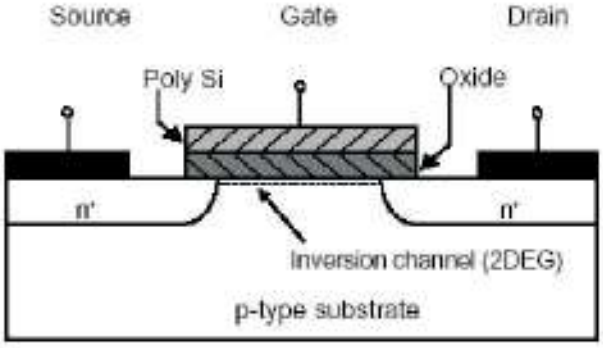

Figure 6: Schematic of a typical bulk n-MOSFET structure with poly- Si gate (F. Schwierz *et al.*, 2003).

Figure 7 shows a bulk implementation of the ground plane structure, using retrograde doping (R. H. Yan *et al.*, 1991). This is basically a bulk MOSFET with carefully engineered substrate doping profiles. A highly doped region, a pulse-shaped doping region, just below the channel is used to mimic the ground plane. From the results, it has been observed that the vertically engineered doping profile preserves the subthreshold behaviors obtained by bulk structures with high doping, but without suffering the speed degradation due to high junction capacitance or

reduced mobility. Through vertical engineering, devices can be designed to improve the standby power consumption and speed trade off, which are essential for scaling gate into the 0.1 pm regime.

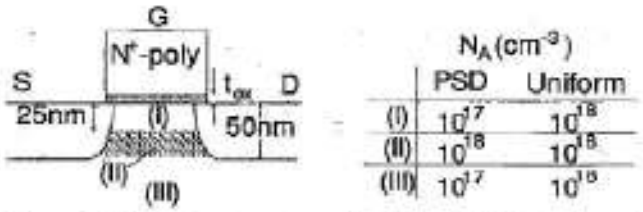

Figure 7: Device structures in bulk Si: Pulse-shaped doping (PSD) and uniform doping. The doping levels are indicated for these two cases at right, and the gate oxide thickness (t_{ox}) is 4 nm (R. H. Yan *et al.*, 1991)

B.2 SOI and Other Device Structures

A somewhat significant modification to the MOSFET during the last 33 years was the introduction of the silicon on insulator (SOI) technology, where the transistor body is separated from the semiconducting wafer by an insulating layer. The gate length, which is directly related to the effective channel length or the feature size of MOSFET, is the main feature controlling the MOSFET performance. Reducing the gate length, however, requires the scaling of other features, such as, the oxide thickness, drain/source junction depth, and substrate doping density. For example, when the gate length is reduced, the oxide thickness needs to be reduced so that the gate can have a better control of the channel inversion and can give rise to a larger oxide capacitance. The device miniaturization rule is shown in Table 1.

Table 1: Road map of MOSFET minimum feature size (M. H. Bhuyan, 2011)

Year	1999	2001	2002	2004	2006	2009	2010	2011	2014
L (nm)	180	130	90	65	45	38	32	22	20
t_{ox} (nm)	~4	~3	~2	~1.5	~1.5	~1.5	~1.1	~1.0	-
					with High-k/Metal gate				

Typically, the gate is made of a heavily doped poly-silicon, and silicides are frequently deposited underneath the drain/source contacts to reduce the contact resistance. Unfortunately, an important phenomenon associated with the short-channel transistor is the threshold voltage roll-off. (i.e., threshold voltage decreases as the channel length reduces below a critical value). Such undesirable effect is called short channel effects (SCE). To alleviate this effect, several additional features have been added to the basic MOSFET structure.

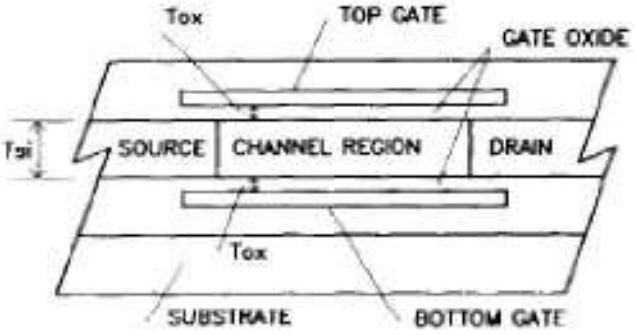

Figure 8: Schematic cross-sectional structure of an XMOS transistor with an additional bottom gate (T. Sekigawa *et al.*, 1984)

The first article on the double-gate MOS (DGMOS) transistor was published in 1984 (T. Sekigawa *et al.*, 1984). They showed that significant reduction of short-channel effects may be obtained by sandwiching a fully depleted SOI layer between two gate electrodes connected together. The device was called XMOS because its cross section looks like the Greek letter (Xi) as shown in Fig. 8. Using this configuration, a better control of the channel depletion region is obtained than in a regular SOI MOSFET. In particular, the influence of the drain electric field on the channel is reduced, which reduces short-channel effects. It is expected that the threshold voltage decrease is less when the silicon layer thickness T_{Si}, is smaller, only when the following inequality holds-

$$T_{Si} < 2\sqrt{\frac{4\varepsilon_{Si}\phi_F}{qN_A}} \text{ ,where } \phi_F = \frac{kT}{q}\ln\frac{N_A}{n_i}$$

In 1987, Balestra *et al.* discovered another important property of double-gate MOSFETs called volume inversion. It is a phenomenon that appears in very thin (or narrow) film multi-gate SOI MOSFETs due to the fact that inversion carriers are not confined near the Si/SiO_2 interface, as predicted by classical device physics, but rather at the center of the film. Volume inversion was first observed in Gate-All-Around (GAA) MOSFETs in 1990. The original GAA MOSFET had a poly-silicon gate electrode wrapped around the entire channel region. Thus in GAA MOSFET, current flows along all four surfaces of it (E. Leobandung *et al.*, 1997). Because the width of the device is much larger than the silicon film

thickness, the original GAA device was really a double-gate device. It is shown in Fig. 9 (J. P. Colinge *et al.*, 1990).

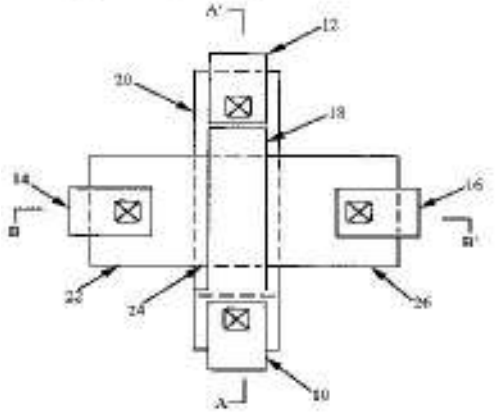

Figure 9: Schematic of GAA MOSFET (J. P. Colinge *et al.*, 1990)

In 1989, Hishamoto *et al.* proposed a fully DEpleted Lean channel TrAnsistor (DELTA) having a new gate structure and vertical ultra-thin SOI structure with selective field oxide. The DELTA transistor was the first multigate transistor, and dynamic random access memory cells based on DELTA devices were reported two years later (I. Ferain *et al.*, 2011). In the deep-submicron region, selective oxidation is useful for achieving SOI isolation. It provides a high quality crystal and Si-SiO_2 interface as good as those of conventional bulk single crystal devices. Using experiments and simulation, it was shown that the new gate structure of DELTA has effective channel controllability and its vertical ultra-thin (<0.2 pm) SOI structure provides superior device characteristics. e. g. the reduction of short channel effects, minimized sub-threshold swing and high trans-conductance. It is shown in Fig. 10 (D. Hisamoto *et al.*, 1989).

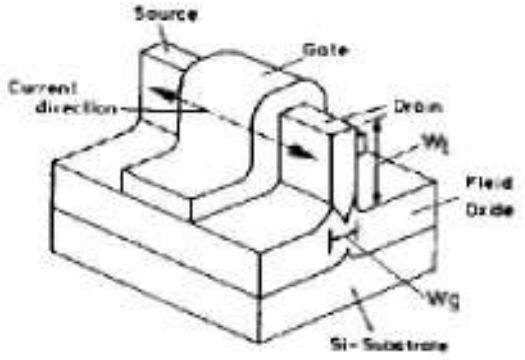

Figure 10: Schematic cross section of DELTA (D. Hisamoto *et al.*, 1989)

In 1992, a high performance Si MOSFET design using dual gate FET has been proposed (as shown in Fig. 11) to be scaled down to the gate lengths of the order 30 nm. Such devices were found suitable for digital logic circuitry, and may have trans-conductances as high as 2300 mS/mm and ring oscillator speeds near 1 ps found by Monte Carlo simulation method. The technology needed to do this includes thickness control of very thin layers, dual gate alignment, very abrupt doping profiles and gate work function control. The international technology roadmap for semiconductors (ITRS) describes three different devices with different power delay tradeoffs: high performance, low operating power (LOP), and low standby power (LSTP). The LOP and LSTP devices are optimized in a similar manner, although the LSTP device has more stringent leakage constraints (S. Hanson *et al.*, 2008).

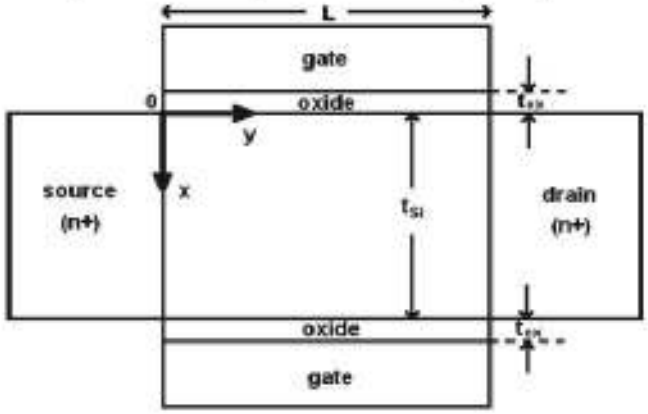

Figure 11: Schematic cross section of Dual Gate MOSFET (A. Tsormpatzoglou *et al.*, 2008).

It has been observed that the DGMOSFET inverter power-delay-product (PDP) is approximately 70% lower than the bulk CMOS inverter and 65% lower than the pseudo NMOS inverter. Other logic gates based upon DGMOSFETs have 30-40% better energy efficiency (lower PDP) than equivalent bulk CMOS logic gates in the subthreshold operation, due to the advantages of DGMOSFETs (R. Vaddi *et al.*, 2011).

In 1998, Hishamoto *et al.* proposed a novel folded-channel MOS transistor to improve the short channel effect for deep sub-tenth micron era. The vertical double-gate SOI type MOSFETs simplified the fabrication process. Special features of this structure are:

1. A transistor is formed in a vertical ultra-thin Si fin and is controlled by a double-gate;

2. Two gate lengths are self-aligned to the S/D;
3. S/D is raised to reduce parasitic resistance;
4. New low temperature gate or ultra-thin gate dielectric materials can be used because they are deposited after the S/D; and
5. The structure is quasi-planar due to relatively short Si fins.

The structure of this transistor is shown in Fig. 12 (E. Hisamoto *et al.*, 1998).

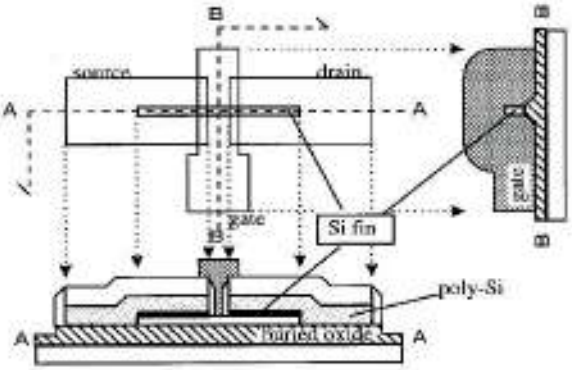

Figure 12: Folded channel MOSFET device structure. The bottom is A-A and the right is B-B cross sections (E. Hisamoto *et al.*, 1998)

A novel device architecture called SON (Silicon On Nothing) is proposed in 1999 that allows extremely thin buried oxides and Silicon films to be fabricated as shown in Fig. 13 (M. Jurczak *et al.*, 1999), and thus resists SCE and DIBL better. SON devices are shown to present excellent I_{on}/I_{off} trade-off, V_{th} roll-off suppression down to 15 nm channel length, and to be free from the short comings of self-heating, high S/D series resistances etc. Expensive SOI substrates as SON devices are fabricated on bulk Si.

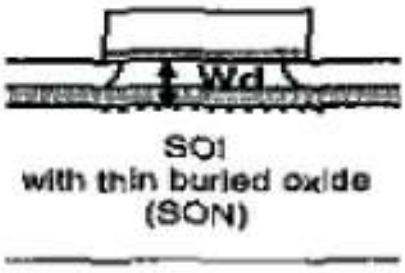

Figure 13: SON device architecture (M. Jurczak *et al.*, 1999)

Invented in 1999 and patented in 2001 by Advanced Micro Devices Inc., the pocket implanted MOS is an improved semiconductor device that shows a delayed threshold voltage roll-off and short channel effects, making the semiconductor devices more tolerant of gate variations for short gate length devices. The invention provides a semiconductor device with an asymmetric channel doping profile. A first pocket dopant implantation with a 0° tilt is used to create a first source dopant pocket and a drain dopant pocket. A second pocket dopant implantation with a 30-60° tilt creates a second source dopant pocket without creating an additional drain dopant pocket, thus creating the asymmetric doping profile. This is shown in Fig. 14 (E. Quek, 2005).

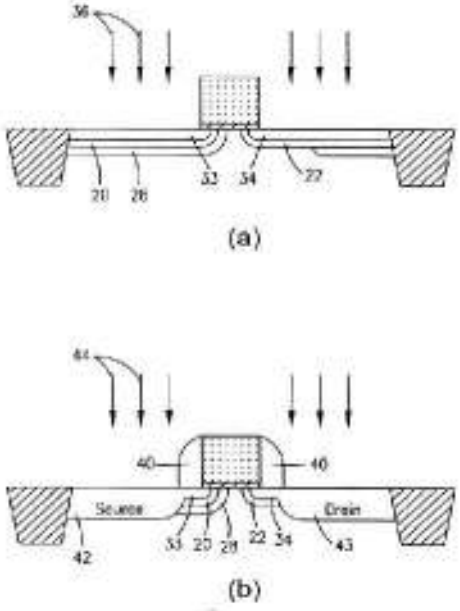

Figure 14: Pocket implanted n-MOSFET structure (E. Quek, 2005)

A new SOI device, the MOS-JFET, as shown in Fig. 15, has been developed combining two transistors, JFET and MOSFET, superimposed in a single silicon island so that they share the same body (B. J. Blalock *et al.*, 2002.). A unique attribute of the MOS-JFET is that it can be viewed as a four-gate (4-G) transistor (two side junction-based gates, the top gate, and the back gate activated by SOI substrate biasing). Each of these four gates can control the conduction characteristics of the transistor. The G4-FET can operate as a high-gain MOSFET with surface channels and as a low-noise JFET with a conducting channel in the semiconductor bulk. In the JFET mode, the conductive region in the bulk is surrounded by depleted regions, which is favorable for radiation-hardened, low-power, high-mobility, and low-noise applications (K. Akarvardar, *et al.*, 2005).

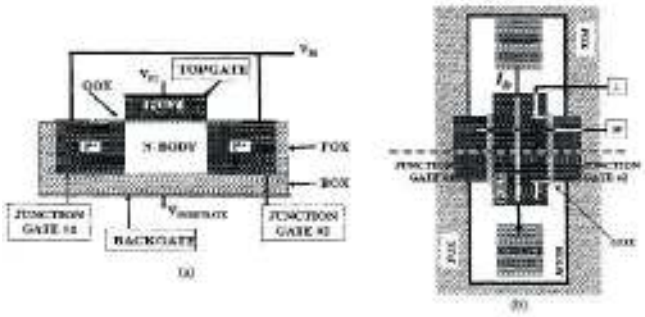

Figure 15: MOS-JFET structure: (a) cross-section and (b) top view (B. J. Blalock *et al.*, 2002.).

To minimize hot-carrier effects due to the high electric field near the drain junction, lightly doped drain/ source (LDD) regions are implemented in MOSFETs. SCE can be effectively eliminated by the use of halo or pocket-implant MOSFET. Many foundries, including IBM, Intel, TSMC, Philips, Motorola, and LSI Logic started volume production of 100- to 90-nm technology node processes in early 2003. In these processes, gate lengths can be selectively etched down to about half this technology node. The primary aim of the entire research and development efforts in VLSI electronics has been to decrease the cost per logic function and per stored bit, and simultaneously to increase the switching speed of logic gates. So far this aim has in fact been achieved and resulted in new generations of microchips containing more transistors and having a higher clock frequency than their predecessor.

B.3 RF MOSFET

An important measure of RF transistor is the cutoff frequency, f_T. This is the frequency at which the small signal current gain h_{21} of the transistor rolls off to unity (i.e., 0 dB). Figure 16 shows the cutoff frequency versus the gate length of n-channel MOSFETs. For 50- to 100-nm gate-length MOSFETs, the cutoff frequency reached an astonishing value of 200 GHz (H. S. Momose *et al.*, 2001). Applying a frequently used rule of thumb that the cutoff frequency should be around 10 times the transistor's operating frequency, one could use these devices to design integrated circuits operating up to 20 GHz, an operating frequency higher than that for the great majority of modern RF electronic devices. However, only a high cut-off frequency is not the only requirement for a good RF transistor. Other figures of merit have to be considered as well. For example, a high maximum frequency of oscillation f_{max} which is the frequency at which the transistor's unilateral power gain rolls off to unity (i.e., 0 dB), is often desirable. Minimum noise figure, NF_{min} and high output power, P_{out} are also critical for RF noise and power applications respectively.

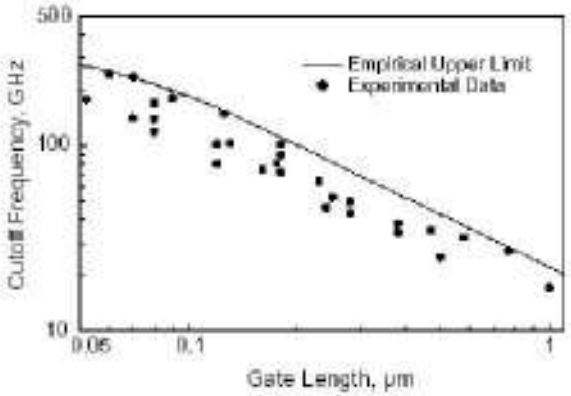

Figure 16: Reported cutoff frequency versus gate length of MOSFETs (J. J. Liou *et al.*, 2003)

Properly designed III–V RF Field Effect Transistors (MESFET and HEMT) show comparable f_{max} and f_T, but typically with $f_{max} > f_T$. The situation is different for Si MOSFETs. For these devices, one could either realize short-channel transistors for high f_T but substantially lower f_{max} or long-channel transistors for rather low f_T but higher f_{max}. So, trade-off is needed using Si MOSFETs. It is reported that the tradeoff resulted from the fact that a very high f_{max} can only be achieved with transistors having a high f_T and a low gate resistance, R_G. For III–V FETs, metal gates with multi-finger mushroom structures are frequently used to minimize R_G. The gates of Si MOSFETs are made of poly-silicon, which has a much higher resistivity than a metal. Reducing R_G is imperative for RF MOSFETs because R_G not only limits the power gain attainable at a certain frequency (and thus f_{max}), but also sets a lower limit to the minimum noise figure. There are several means to minimize the gate resistance of Si MOSFETs, such as,

1. Deposition of silicide on top of the poly-silicon gate,
2. Metal over gates on top of the poly-silicon gates,
3. Multi-finger gates with small finger width.

Recently, considerable progress on increasing the maximum frequency of oscillation of Si MOSFETs has been made. Reported maximum frequencies of oscillation are: f_{max} of 193 GHz (f_T of 178 GHz) for the 50-nm SOI-MOSFET (S. Narashima *et al*., 2001) and f_{max} of 185 GHz (f_T of 120 GHz) of the 80-nm SOI-MOSFET (T. Hirose *et al*., 2001). Because of the presence of Si/SiO_2 interface, MOSFETs are noisier than other RF transistors. Reported minimum noise figures NF_{min} of experimental Si MOSFETs were found around 1.5 dB at about 15 GHz (F. Schwierz *et al*., 2003), and MOSFETs become too noisy at even higher frequency for practical microwave applications.

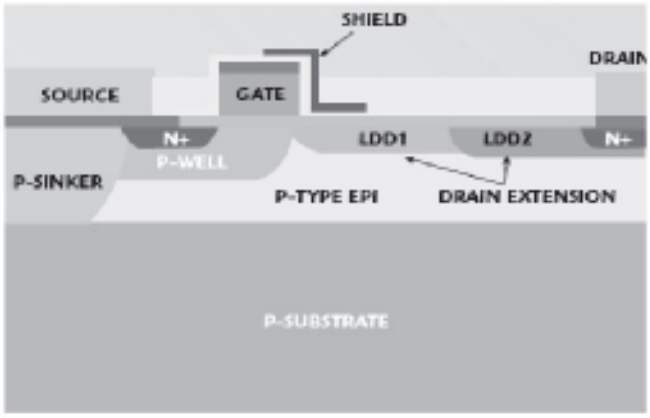

Figure 17: Typical cross-section of a state-of-the-art LDMOS technology (P. C. A. Hammes *et al*., 2004)

High-power microwave amplifiers used in the base stations for mobile communication systems, however, are designed for maximum operating (and thus breakdown) voltage to deliver maximum output power. For such applications, a different structure called the laterally-diffused MOSFET (LDMOSFET) is frequently used. The cross-section of a typical high-power LDMOSFET is shown in Fig. 17 (P. C. A. Hammes *et al*., 2004). It consists of a p^+-Si substrate on top of a lightly doped p^--layer grown epitaxially. While the n^+-source region extends to the gate, the n^+-drain region is spatially separated from the gate. The conductive connection between the n^+-drain and the channel region underneath the gate is realized by an n^--LDD (lightly doped drain) region which is frequently called the drift region. This is the main region contributing to a high breakdown voltage. Typical gate length of LDMOSFETs is in the range of 0.3-1.0 pm and the gate oxide is several nm thick. As such, the technology, especially, the lithography and the gate oxide deposition, of the LDMOSFET is much more relaxed than that of the small signal microwave MOSFETs. Depending on the specific designs, typical f_T of LDMOSFETs is around 5-15 GHz, and the drain-to-source breakdown voltage BVDS is around 20-40 V.

C. Future trends

C.1 Mainstream CMOS

The road to advances beyond a decade into the future has always been obscure and has stimulated much speculation as to where miniaturization must end. Thus far, new ideas have regularly met the challenges posed by new problems. One thing for sure is that the downscaling will continue at least for a couple of years. The ITRS has already targeted in the year 2016 for high performance logic circuits (microprocessors in desktop computers) that the physical MOSFET gate length (i.e., the transistor's gate length after all fabrication steps are finished) would be of 9 nm and microprocessors with a chips size of 140–280 mm^2 containing more than 3 billion transistors.

To reach this target and ensure that the transistor still operates satisfactory, however, requires many changes and innovations. The most likely changes are:

(a) To increase the mobility and improve performance, silicon will be mixed with a semiconductor like germanium to produce a strained mono-crystalline silicon layer at the wafer surface that lets electrons move faster.

(b) To reduce the gate leakage current, gate oxide will be made of materials with higher dielectric constant than today's silicon dioxide.

(c) To reduce the gate resistance and improve channel control, gates will be made of metals, instead of poly-silicon.

(d) For better control of MOSFET's on and off states and reduce power consumption, more than one gate will be used.

The technology of putting a Si strained layer on a silicon wafer seems very promising. In this case, Germanium atoms replace some of the silicon atoms near the wafer's surface, then a thin layer of silicon is grown on top of this SiGe layer. Because Ge atoms are larger than Si atoms, the distance between the atoms in the SiGe layer is

larger than that in pure Si. When the top Si layer is grown, its atoms line up with the SiGe atoms below, and it becomes strained in the two directions parallel to the plane of the wafer. Finally, MOSFETs are fabricated in this top strained silicon layer. The tensile strain forces in the strained silicon layer change the energy band structures. As a result, the effective mass of electrons and holes is reduced and the phonon scattering is decreased. Thus higher free-carrier mobilities in Si strained layer are possible. It is reported that over 100% increase in the mobilities (T. Pešić-Brđanin *et al.*, 2014). Typical strained Si MOSFET structures are shown in Fig. 18.

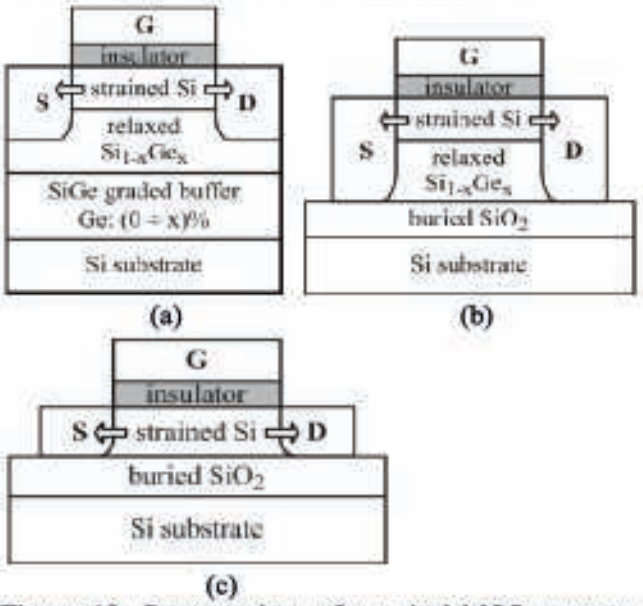

Figure 18: Cross-sections of a typical MOS structures using biaxial strain (T. Pešić-Brđanin *et al.*, 2014)

Besides, there have been researches on the structures with strained silicon layer on insulator (Strain-Si On Insulator - SSOI) (S. Takagi *et al.*, 2001), where strained/relaxed layers are formed on the buried oxide, and the structures where the strained silicon layer is directly linked to the buried oxide (Strain-Si Directly On Insulator - SSDOI) (K. Rim*et al.*, 2003).

The oxide thickness decreases with decreasing gate length. For a 100-nm process, the oxide thickness should be around or even less than 1.5 nm. Such a thin oxide allows for a considerable amount of current to flow from the gate to channel, thereby increasing the power consumption and degrade the functionality of MOSFETs. Thus the concept of using higher dielectric constant (k) material emerges. A gate over a thick high-k material can control the channel just as effective as one over a thinner low-k material. Consequently, using a high-k dielectric allows one to increase the oxide thickness and reduce the gate leakage. Most of the researches for high-k dielectrics are centered on oxy-nitrides and hafnium di-oxide.

Today's MOSFETs have heavily doped poly-silicon gates. When the gates are biased, a depletion region forms near the interface of poly-silicon gate and oxide layer. Since the oxide is very thin, this depletion region in effect increases considerably the thickness of the dielectric and therefore reduces the effectiveness of the controlling mechanism of the gate. The second drawback of poly-silicon gates is their relatively high series resistance. Metal gates can minimize these two problems. But before choosing a suitable metal, factors, such as, thermal stability and work function differences need to be considered seriously. Ruthenium-Tantalum alloy has been suggested as a possible gate metal, which has the advantage of adjustable work function to meet the required threshold voltage of MOSFETs.

In the past few years, extensive research works have been carried out to investigate innovative MOSFETs having more than one gate to enhance the control of ultra-small MOSFETs. Several vertical and planar structures have been suggested and tested, and the frontrunner is an approach called the double-gate MOSFET (DGMOSFET) under development by many semiconductor companies. In Fig. 19, two double-gate MOSFET versions are shown. On the left is a planar double gate transistor investigated by IBM researches, and the other is a vertical double gate FET commonly called FinFET popularized by AMD, TSMC, and others. The FinFET is built by etching the silicon layer of an SOI wafer to form narrow vertical fins on the wafer surface. The narrow fin forms the channel, the source and drain are formed at end of the fin, and the gate drapes over both sides of the fin (i.e., two gates). Since the fin is made extremely thin, no region of the fin escapes the influence of the gate, and no leakage path for the carriers to flow between the source and drain when the device is off.

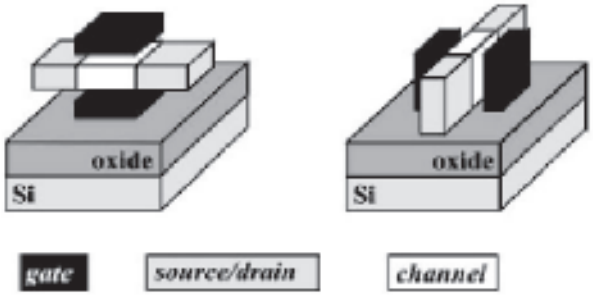

Figure 19: Schematic of a planar double-gate MOSFET (left) and a vertical double-gate MOSFET (FinFET, right) (J. J. Liou *et al*., 2003)

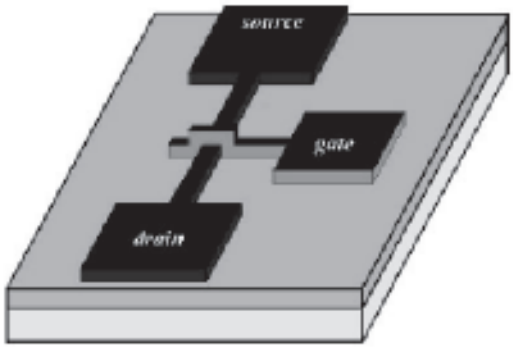

Figure 20: Schematic of a Tri-gate MOSFET (J. J. Liou *et al*., 2003)

Currently, Intel is pushing for a modified FinFET version called the Tri-gate FET. Here, an almost quadratic cross-section of the fins is striven for and the gate surrounds the fin from the vertical surfaces and from the top. Thus, there are three gates controlling the current path in the fin. Such a device is schematically shown in Fig. 20.

Today, nanoscale vacuum channel transistors are being developed. It can operate at less than 10 volts. Once the gap between the emitter and the collector is further reduced to only 10 nm, the power requirements will drop to less than a watt, which would be competitive with modern semiconductor technology. It can be manufactured using standard silicon semiconductor processing, can operate at high speeds and could consume just as much power as a standard transistor. In semiconductors, electrons speed is limited to about 10^7 cm/s, but in the vacuum they can travel at almost 10^{10} cm/s, the speed of light, i.e., around 1000 times faster than conventional channel transistors (J.-W. Han *et al*., 2012). Its few structures are shown in Fig. 21.

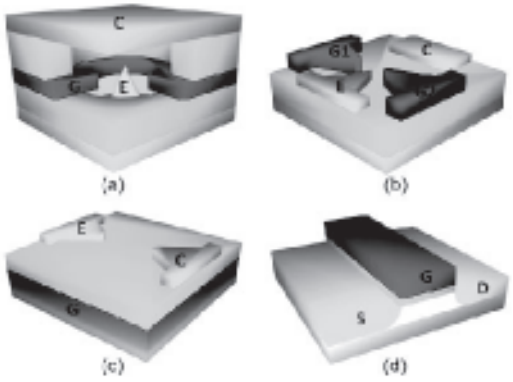

Figure 21: Structures of vacuum channel devices and analogous to conventional MOSFET. (a) Vertical field-emitter, (b) planar lateral field-emitter, (c) MOSFET, and (d) gate-insulated air channel transistor (J.-W. Han *et al*., 2012)

Besides, research on Double Metal Double Gate (DMDG) MOSFET, Tipple Metal Double Gate (TMDG) MOSFET, Tunnel FET (TFET), Carbon Nano Tube FET (CNTFET), Nano Wire FET, Negative Capacitance FET, 2-D Channel FET etc. are going on. These transistor structures are most promising for research. Because, they offer many more advantages and have shown great improvement of performances.

C.2 RF MOSFET

The advanced MOSFET concepts described above are focused on developing transistors for high-level integrated circuits, such as microprocessors, ASICs, etc.

In the past, the preferred RF MOSFET structures were conventional single-gate bulk or single-gate SOI MOSFETs. There is no doubt, however, that RF MOSFETs have been blessed by the tremendous development made in VLSI and ULSI semiconductor industries. Besides, the MOSFET is a good passive on-chip component, i.e. capacitors, inductors, and resistors, which can be made using the CMOS processes. Technical progress in bringing SiGe HBT technology to reality has been exceptionally rapid. The first functional SiGe HBT was demonstrated in December 1987 (S. S. Iyer *et al*., 1987; G. L. Patton *et al*., 1988). Worldwide attention was directed toward the technology in mid-1990 by the demonstration of a non-self-aligned SiGe HBT with a cut-off frequency of 75 GHz (G. L. Patton *et al*., 1990). Recent progress on the SiGe HBT will help to expand the market share of MOSFETs

in RF electronics. SiGe HBTs offer excellent RF properties (high speed, i.e. both high f_T and f_{max} and low noise figure), as evidenced by the noise margin (NF_{min}) given in Table 2.

Table 2: State of the art noise figures of SiGe HBTs

Cut-off Frequency, f_T(GHz)	Noise Margin, NF_{min}(dB)	Reference
2	0.14	H. Schumacher *et al.*, 1997
4	0.18	H. Schumacher *et al.*, 1997
10	0.20	D. R. Greenberg *et al.*, 2002
26	1.50	D. R. Greenberg *et al.*, 2002
278	1.748	O. Esame *et al.*, 2004

During the last few years, considerable reports have been devoted to realize SiGe HBTs from standard CMOS processes. This makes pure Si-based RF ICs possible, where SiGe HBTs are used in the critical parts which demand RF performance (such as frequency and noise performance) while Si MOSFETs are employed in other components. An interesting feature of SiGe HBTs is the fact that both f_T and f_{max} between 50 and 100 GHz can be realized with an emitter width larger than 0.4 □m (J. J. Liou *et al.*, 2003). This is different from the RF Si MOSFET, which requires a much smaller gate length to reach such high frequency limits.

III. Applications of CMOS Technology

There are many technologies available in the semiconductor industry, each adapted to one or several applications. Complementary Metal-Oxide Semiconductor (CMOS) is by far the most popular semiconductor technology in this industry and the choice of mass production for fabricating digital circuits today. In CMOS, components, such as, microprocessors, logic circuits and amplifiers are designed with MOSFETs as building blocks. With CMOS technology, it has been made possible to downscale the MOSFET, which is an appealing property to foundries due to cost-effectiveness and feasibility. In this section, few application areas of CMOS technology will be mentioned.

LDMOSFET technologies have been in the dominant position in the wireless base station applications for frequencies ranging from 450 MHz to 2.7 GHz for more than 20 years due to performance, cost, reliability, and power capability advantages (G. Ma *et al.*, 1996; H. Brech *et al.*, 2003). The operating frequencies of civil RF applications can range from a few hundreds MHz to 100 GHz, but most systems having mass markets operated at frequencies below 6 GHz. As third and fourth generations (3G and 4G) cellular systems, such as, W-CDMA are emerging, the demand for transistors with increased output power has escalated in support of the RF power amplifier designs required for base station infrastructure (C. P. Dragon *et al.*, 2000). The number of units sold in these markets is of the order of billions per year. For pocket implanted MOSFET, reported circuit applications include a 256 M-bit DRAM and Mixed-Signal Processor.

Cellular phones are no doubt the most popular wireless communication system currently in use. In wireless communications, the noise produced intrinsically in the RF devices is somewhat negligible comparing to that from the noisy environment. GaAs MESFETs and Si bipolar transistors as the traditional low-noise transistors used in wireless communications, but the use of MOSFETs, possibly merged with SiGe HBTs using a low-cost BiCMOS process, has become a realistic option. Another requirement for the handset is the reduction of power consumption. At present, a supply voltage of 3 V has been established as a standard. To deliver a high output power combined with a high efficiency at a limited supply voltage of 3 V, RF power transistors possessing a large on-current and a low on-resistance are required in the transmit section of the handset. MOSFETs are not the best devices for this application due to the relatively low output power density. GaAs transistors (especially GaAs HBT) dominate this application. To date, the dominant power RF transistor used in base stations of wireless communications systems with operating frequencies up to 2.8 GHz is the Si LDMOSFET, which in the last several years has replaced all other competing Si and GaAs transistors. Si LDMOSFETs combine the advantages of moderate cost, high reliability and extremely high output power (A. Wood *et al.*, 1996). Aside from cellular phones, several other civil RF systems with operating frequencies below 20 GHz are potential fields for the application of RF MOSFETs as well. For example, Bluetooth, in which the requirements on transistor's RF performance are quite moderate, is predestinated for RF MOSFETs. In fact, all-MOS Bluetooth products are commercially available. For other applications below 20 GHz but with more stringent requirements concerning RF performance, the combination of SiGe HBTs and

CMOS (SiGe BiCMOS) is currently a heavily discussed possibility in industry. Table 3 summarizes various RF applications and their frequency spectrums (J. J. Liou *et al.*, 2003).

Table 3: Civil RF systems operating below 6 GHz

Application	Operating Frequency (GHz)
Pagers	0.2-0.9
Cellular phone (1G)	0.8-0.9
Cellular phone (2G, 2.5 G)	0.9-1.9
Cellular phone (2.5 G)	2.5
Cellular phone (3G)	3.0
GPS	1.8
WLAN	2.4
Bluetooth	2.4
Microwave Oven	2.4
GPRS	2,5
HiperLAN2	5.0
802.11a LAN (Wi-Fi)	5.15-5.825
Collision avoidance RADAR in automobiles	77

Although RF MOSFETs seem to fulfill the most of the performance requirements for civil RF systems with operating frequencies from several 100 MHz up to 6 GHz, debates still existed as to whether such devices will find widespread applications in the market. Nevertheless, the importance of MOSFETs in RF applications is increasing day by day and it will continue to rise in the future.

Four Gate SOI transistor's multiple gate inputs give rise to exciting circuit opportunities for analog, digital, RF, and mixed-signal applications.

Vacuum channel transistors could be used for THz frequency operation, such as, sensing hazardous chemicals, noninvasive medical diagnostics, high-speed telecommunications, as well as in extreme environments having high temperature and various radiations, military and space applications etc.

IV. Conclusions

There is no doubt that MOSFETs are progressing quickly and becoming a strong contender in the RF applications traditionally dominated by III–V devices. Today's RF MOSFETs already fulfill most of the performance requirements for civil RF systems operating in the frequency range up to 6 GHz. Rapid technology advancement, cost and size reduction are promoting extensive applications of MOS devices in residential, industrial, commercial, aerospace, military, transportation and utility systems.

Finally, it can be said that there is still a place for CMOS devices. As long as the performance needed is reached, CMOS will continue to be the choice of technology, but the time is coming where CMOS is difficult to downscale further without affecting the performance and other solutions are being sought after. The impact of new devices on multi-core, von Neumann architectures needs careful study at the architectural-level. Still computationally interesting things with 'imperfect' devices can be done. Mixed signal systems may exploit I-V characteristics, other features of new devices. Spin-based devices offer architectural opportunities and challenges. New device structures are bringing other intangible benefits. Model is very useful for circuit simulation of MOSFETs having channel length in the nano scale regime and for studying and characterizing the advanced ULSI devices. So, modeling of new devices requires knowledge on device geometry and device physics insights.

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