



# Design and Simulation of a 4:1 Multiplexer in Microwind and DSch using 90 nm CMOS Technology

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## Abstract

Now a day, low power and low energy have become an important issue in consumer electronics and it is necessary to do research in combinational circuits. One of the important elements in digital circuits is a multiplexer or data selector for processing multiple inputs with a single output. At present, multiplexers have become a universal logic circuit used to design other combinational logic circuits or digital systems. Therefore, now attention is being given to design or revise the design of a multiplexer topology so that the power consumption and area occupancy become low and at the same time speed becomes high. In this paper, Complementary Metal Oxide Semiconductor (CMOS) logic-based 4:1 multiplexer has been designed, simulated and analyzed in terms of its performance at the transistor level using CAD tools of DSch and Microwind.

**Keywords:** CMOS, Multiplexer, Capacitance, MOS Transistor, Microwind, DSch.

## I. Introduction

A multiplexer is a logic circuit that can select one of many analog or digital input signals and can transfer the designated input information into a single output channel. A multiplexer of  $2^n$  inputs has  $n$  number of data selection lines, which are used to pick the desired input channel for transmitting the binary data to a single output channel. This type of logic circuit is mainly used to increase the amount of data that can be transmitted through a digital system or circuit during a given time period and channel bandwidth (M. M. Mano and R. Kime, 2001; S.-M. Kang and Y. Leblebici 2003; N. Weste and D. Harris, 2004). This is also termed a data selector, as it can select a particular signal from a definite number of channels each containing data to pass to another device. A multiplexer is an indispensable constituent in digital system design. It is widely used in data route demanding designs. Data selectors can be considered as a multiple-input and single-output switch. The control/select input lines connect the desired input channel to the appropriate output channels (T. L. Floyd, 2011).

At present, multiplexers have become a universal logic element used to design any digital combinational logic circuits/systems in integrated circuit design so it is needed to design or revise a multiplexer topology for surface area reduction, low power consumption and high speed operation,

i.e. reduced propagation delay. In 8-bit Carry Skip Adder (CSA) and Carry Select Adder (CSA) circuits, the carry is selected by the multiplexer (A. S. Ramya *et al.*, 2015).

CMOS technology is being used to design high speed compact logic circuits since early 80s' (R. H. Krembec *et al.*, 1982). In CMOS logic design, half of the power is dissipated in pMOS and stored energy is dissipated throughout the discharging process of output load capacitor. The energy taken from the power supply is not used fully and half of the energy is dissipated as leakage (P. Saini and R. Mehra, 2012). In order to reduce surface area, to increase the energy efficiency and power dissipation of the logic circuits, CMOS technology at various nodes are being used to design various logic circuits (S. N. Wooters *et al.*, 2010; A. M. Shams *et al.*, 2002; M. A.-Hernande and M. L.-Aranda *et al.*, 2011).

Therefore, in this paper, a 4:1 multiplexer has been designed using CMOS-based digital logic circuit and analyze its performance parameters.

In the subsequent section of this paper, we will review the literature, then we will derive the theoretical development of work, then we will describe the design and simulate our circuit, after that we will present the results and discuss on various aspects of the simulation results. Finally, we will conclude with some recommendations.

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## II. Literature Review on Multiplexers

Low power, high speed and area-efficient design for digital gadgets are fundamental requirements of digital circuits that used in VLSI. A multiplexer is a primary cell for every digital circuit. In this paper, we report on design and simulation of a 4:1 multiplexer using CMOS.

With the conventional transistors, the chip manufacturers are facing a lot of problems. Leakage current is one of them (). Due to the shrinking of transistor's size, off-state current ( $I_{off}$ ) that flows through the channel of the transistor when the device remains idle and no voltage is applied on the gate, has increased steadily (M. H. and Q. D. M. Khosru, 2010). However, a change in the device structure would reduce this impact of CMOS scaling (M. H. Bhuyan, 2011; M. H. Bhuyan, 2017). Thus power is wasted as heat energy causing the CPU to become hot requiring extra power for the cooling fan to dispose extra heat from the system and hence needs further power. Another problem of the conventional transistor is the voltage reduction with chip size reduction. We know that threshold voltage ( $V_{th}$ ) is required at the gate to switch the transistor on. In each generation of CPUs, this  $V_{th}$  has declined because of the reduction of the transistor size though the structure modification can reverse this phenomenon (M. H. Bhuyan and Q. D. M. Khosru, 2010). But the applied voltage hasn't been scaled down proportionately with the size of the transistor (M. H. Bhuyan, 2017). This has created a difficult situation as the power used by the chip is directly proportional to the square of the applied voltage. That means, more transistors are being switched ON/OFF in a comparatively smaller area. Thus the power density of the chips have increased manifold, and thus keeping the chips cool became challenging than before and hence increasing the complexity of the modern CPU's cooling systems (M. H. Bhuyan, 2017).

Short Channel Effects (SCE) arises due to the threshold voltage reduction with the shortening of channel length of the FET. The alternative way is to find new architectures of the transistor. Using additional layer of pockets in the channel region at the source/drain ends might provide a better solution to eradicate this problem through exhibiting Reverse Short Channel Effect (RSCE) (M. H. Bhuyan, 2011, M. H. Bhuyan, 2017).

An automatic logic/circuit synthesizer was designed with basic composing cells from the pass-transistor cell library containing 2:1 multiplexers and inverters. It creates efficient binary decision diagrams whose nodes are realized by using a 2:1 multiplexer for these Boolean functions. It took less response time and surface area (S.-fu Hsiao *et al.*, 2002).

Design and analysis of high performance 2:1 multiplexer circuit was proposed for digital system applications and demonstrated the supremacy in the form of power-delay product, temperature and frequency stability using 90 nm and 45 nm CMOS technology (I. Gupta *et al.*, 2011; I. Gupta *et al.*, 2012).

A purely multiplexer based high speed barrel shifter VLSI circuit was designed and realized in 0.6  $\mu\text{m}$ , n-well CMOS design method based on three diverse design styles of logic based circuits, such as, optimized static CMOS, transmission gate (TG) CMOS and dual rail domino CMOS logic and thus the propagation delay maintaining around same average power consumption was reduced. (A. Asati and C. Shekhar, 2012).

An 8-bit Arithmetic Logic Unit (ALU) was designed based on 16:1 multiplexer using Verilog HDL and was demonstrated as more efficient, less power-intensive, fewer surface-area occupancy and faster speed concerning for the conventional ALU. Of course, only 9 out of 16 inputs were used for ALU operations (S. Rajput, 2013).

A full adder circuit designed using multiplexer was proposed based on 180 nm CMOS process model at the supply voltage of 2.5 V. The SPICE simulation results show that the new circuit's achievement is superior when some parameters speed, power ingesting and power-delay product are measured (V. K. Pandey and R. Kumar, 2014).

In an article, FPGA architecture based 2:1, 4:1 and 8:1 multiplexer designs were proposed (B. Samiksha and M. Sathish, 2015). These were used for various logic operations. However, FPGA based architectures are not so efficient than CMOS based architecture.

Another 2:1 multiplexer design was presented using several logic styles, viz., Differential Cascode Voltage Switch Logic (DCVSL), Modified Differential Cascode Voltage Switch Logic (MDCVSL), CMOS Logic and Pseudo nMOS Logic. Then they analyzed it by using the

Tanner EDA tool and finally claimed that the Pseudo nMOS logic design takes the lead with respect to the other design styles of 2:1 multiplexer if power consumption of the circuit is taken into consideration (S. Abirami *et al.*, 2015).

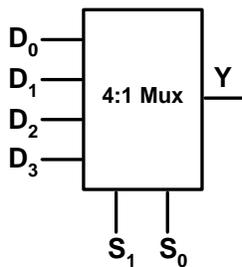
Performance was analyzed of a 4:1 multiplexer circuit using 0.18  $\mu\text{m}$  CMOS technology based on Positive Feedback Adiabatic Logic (PFAL), Cascode Voltage Switch Logic (CVSL) and Transmission Gate based Logic (TGL) styles (M. Sumathi *et al.*, 2016).

The objectives of this project/ research are-

- Design a circuit of 4:1 multiplexer using CMOS transistors.
- Extract the layout of the circuit for simulation and analysis purpose.
- Simulate the designed circuit in simulation tools and find out its output results.
- Analyze its performance considering power supply, current drawn and speed of propagation in 90 CMOS technology node.

### III. Development of Multiplexer Circuit

A multiplexer is a device that has many inputs and one output. The selected line decides which input is going to be connected to the output line. The block diagram of the designed 4:1 multiplexer is depicted in Fig. 1.



**Figure 1:** Block diagram of 4:1 multiplexer (T. L. Floyd, 2011)

A 4:1 multiplexer comprises four data input lines as  $D_0$ ,  $D_1$ ,  $D_2$  and  $D_3$ ; two select input lines as  $S_0$  and  $S_1$  and an output line as  $Y$ . The selector lines  $S_0$  and  $S_1$  select one of the four input lines ( $D_0$  through  $D_3$ ) and associate it to the output line,  $Y$  depending on combination of data of  $S_0$  and  $S_1$  as per Table 1. Fundamentally, this can be described by employing a Boolean equation. The Boolean expression ( $Y$ ) for the 4:1 multiplexer with data input lines  $D_0$  to  $D_3$  and data selection lines  $S_0$  and  $S_1$  are given by equation (1).

$$Y = D_0\bar{S}_1\bar{S}_0 + D_1\bar{S}_1S_0 + D_2S_1\bar{S}_0 + D_3S_1S_0 \quad (1)$$

The truth table of a 4:1 multiplexer from the Boolean equation (1) is shown in Table 1 in which four input combinations 00, 01, 10 and 11 on the select lines ( $S_1S_0$ ) switches the inputs  $D_0$ ,  $D_1$ ,  $D_2$  and  $D_3$  to the output  $Y$  respectively.

**Table 1:** Truth Table of a 4:1 Multiplexer

$S_1$	$S_0$	$Y$
0	0	$D_0$
0	1	$D_1$
1	0	$D_2$
1	1	$D_3$

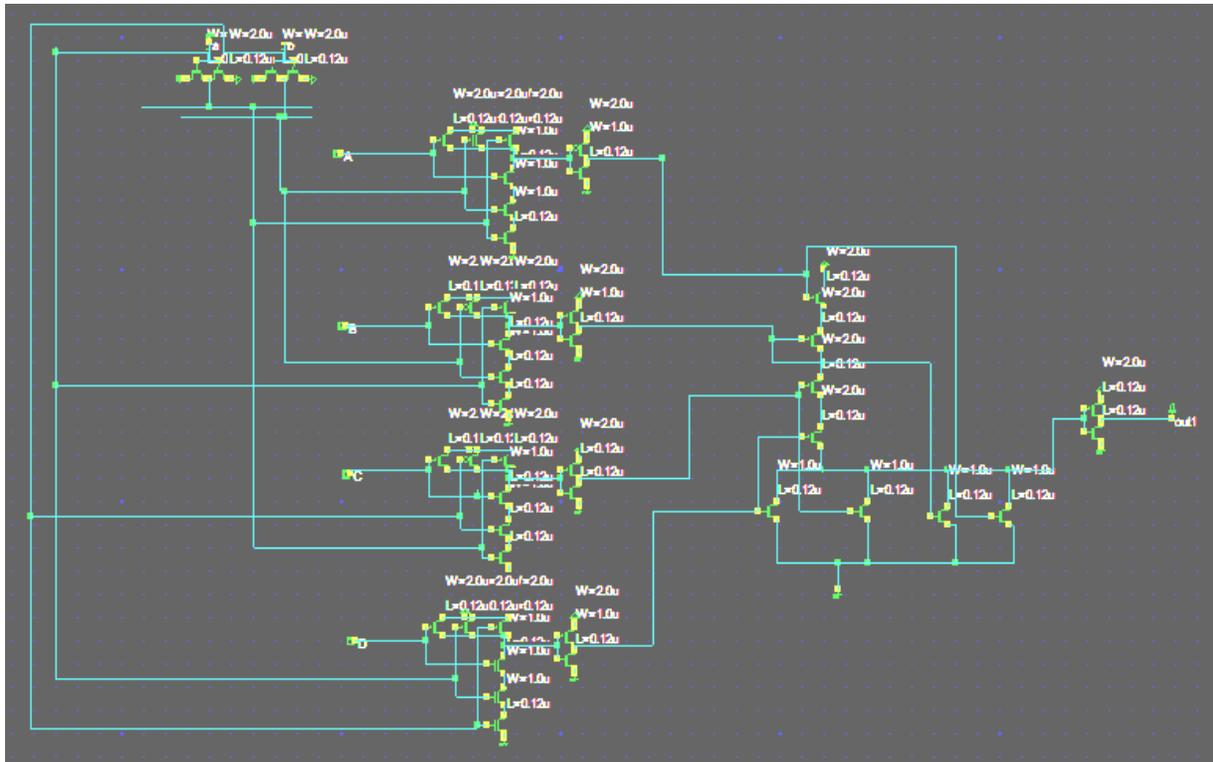
By the term electronic switch, we mean an electronic component that has the capability to stop or pass a certain level of a signal from the input to the output side. The solid-state switch comprises either a pMOS transistor or an nMOS transistor or both. When both transistors are in a same circuit then it works in complimentary fashion and that is why it is called CMOS switch. Here both pMOS and nMOS transistors work simultaneously. Complementary Metal Oxide Semiconductor (CMOS) technology is used to manufacture the integrated circuits (ICs), such as, digital logic gates and circuits, microprocessors, microcontrollers, digital signal processors, digital memory devices, HDDs, Flash Drives, static and dynamic RAMs, ROMs, EPROMs, EEPROMs etc. The foremost advantages of CMOS technology are compact area based design, small amount of static power consumption and low level of noise margin. It requires almost no electrical current apart from its time of altering from one level to another (M. H. Bhuyan, 2017).

### IV. Simulation Results and Discussions

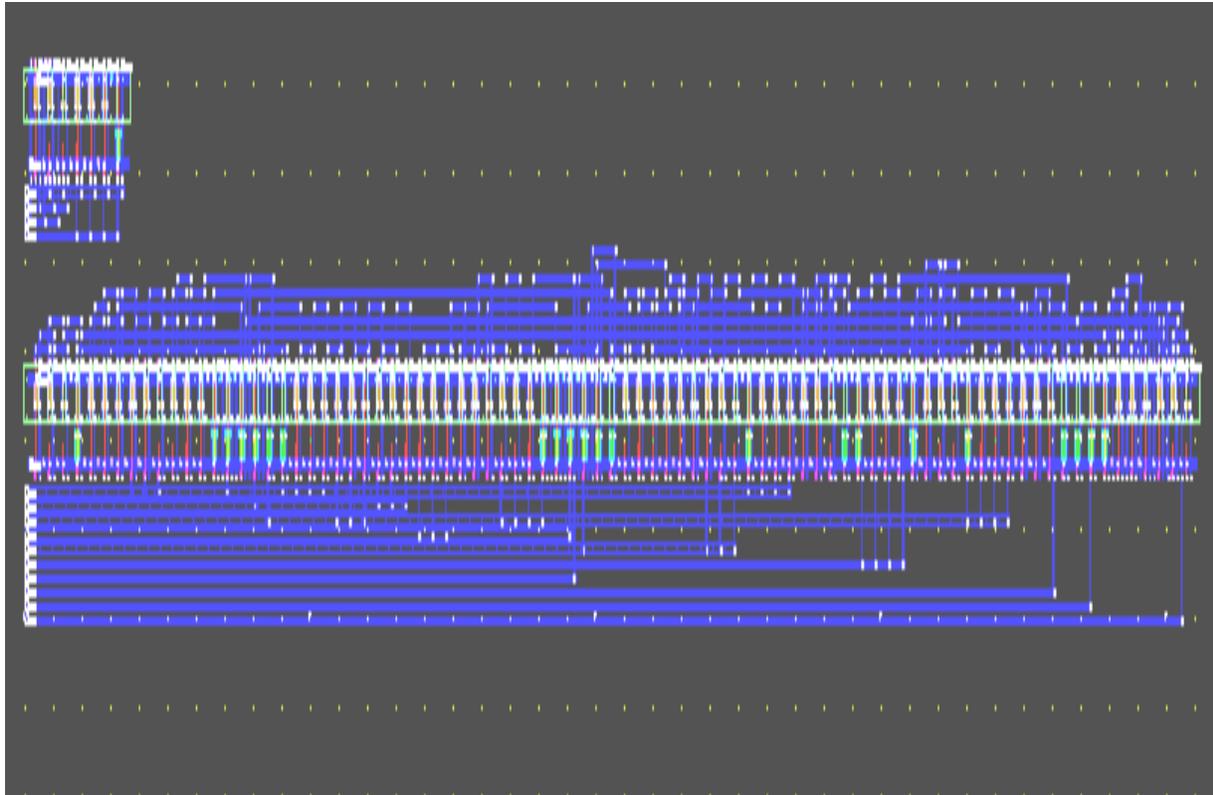
To do this design, simulation and analysis, two software tools have been used. The circuit is designed using 90 nm CMOS process in DSch software and then layout is extracted. A Verilog file has been created from the simulation of this design file. After that the simulation of layout diagram is performed in Microwind software (Aziz *et al.*, 2010) to analyze the performance of the designed circuit.

The designed circuit of the 4:1 multiplexer developed in DSch software (DSCH, 2019) is shown in Fig. 2.

Layout diagram of a 4:1 multiplexer circuit extracted from DSch using 90 nm CMOS process in Microwind is given in Fig. 3.



**Figure 2:** Layout Diagram of a 4:1 multiplexer using 90 nm CMOS technique in DSch



**Figure 3:** Layout diagram of a 4:1 multiplexer using 90 nm CMOS in Microwind

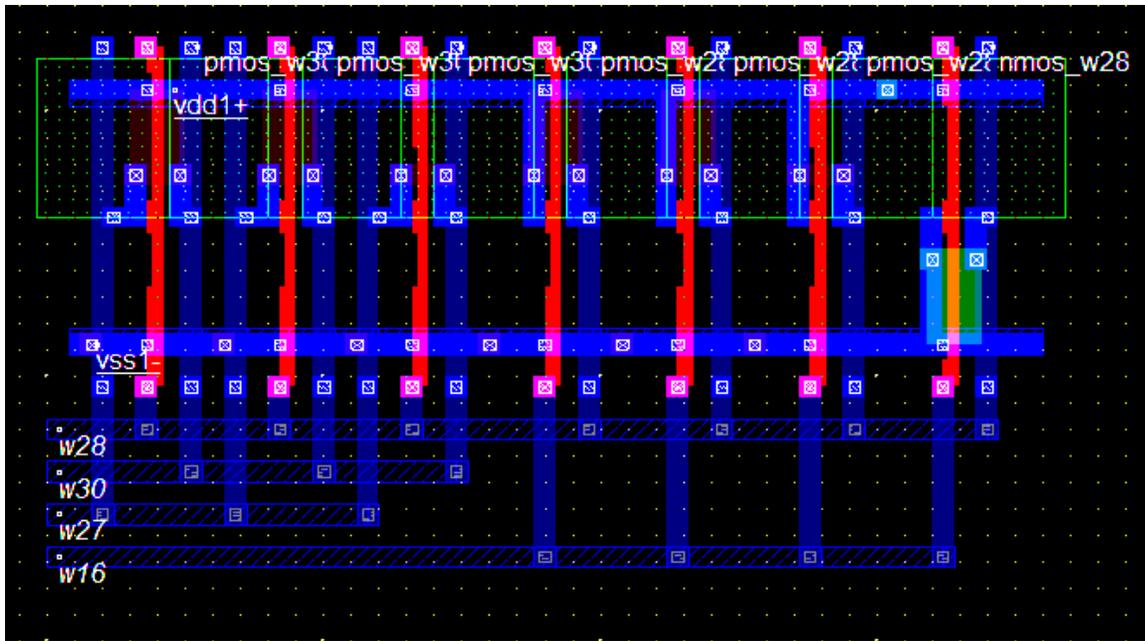


Figure 4: Portion of layout diagram of 4:1 multiplexer using 90 nm CMOS in Microwind

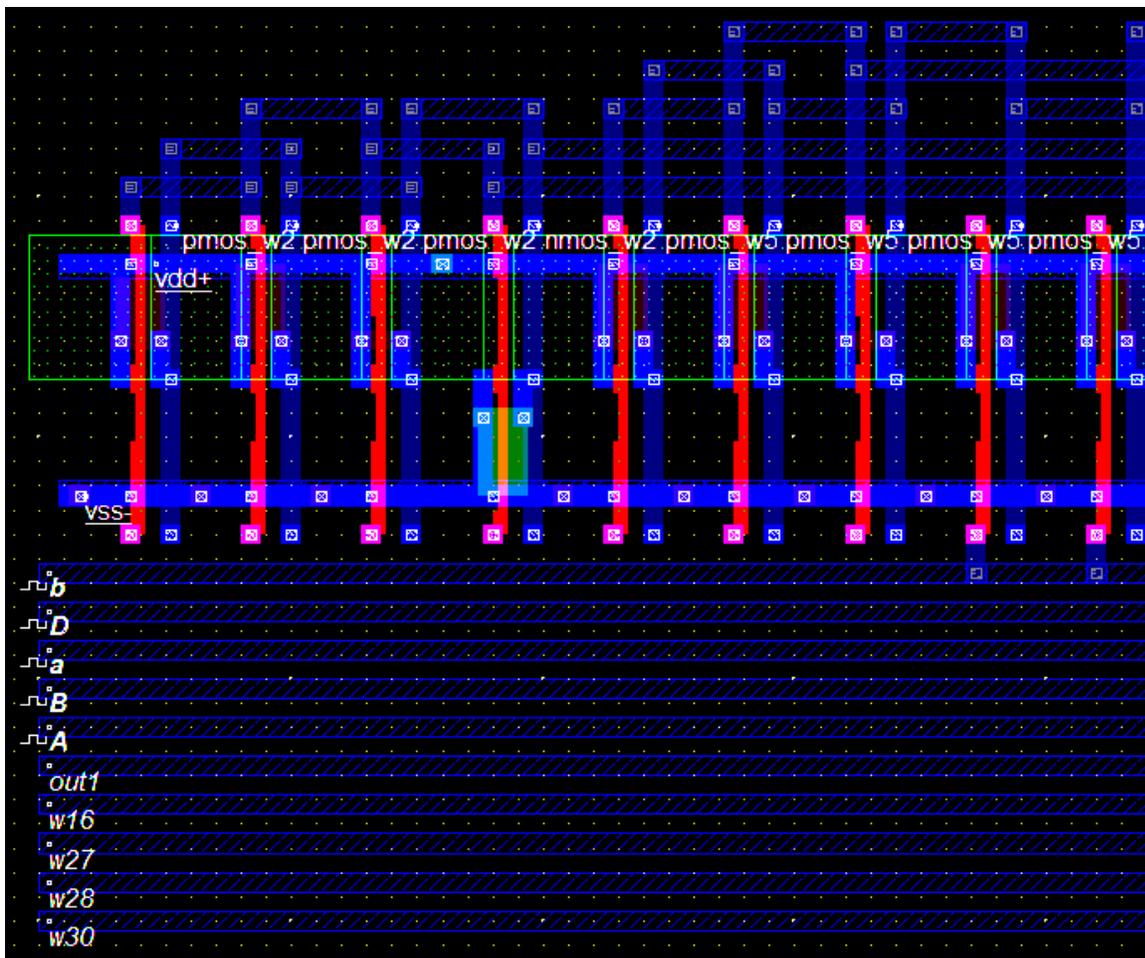


Figure 5: Portion of layout diagram of 4:1 Multiplexer

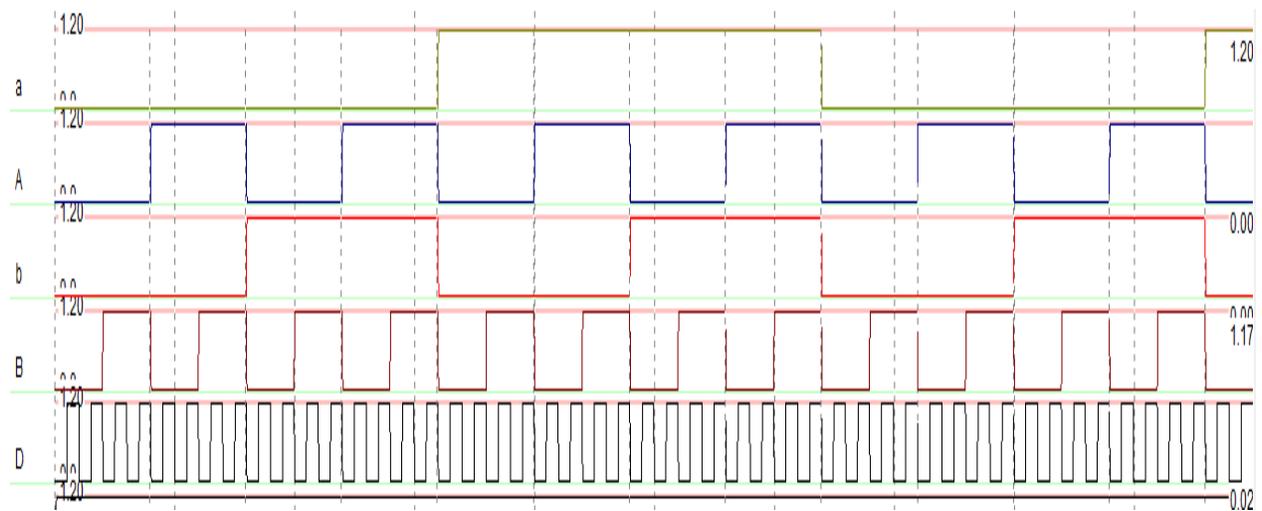
In this paper, the digital circuit 4:1 mux was implemented by a low power technique namely CMOS. Simulation parameters of the designed circuit have been presented in Table 2.

**Table 2:** Simulation parameter values

Supply voltage	1.2 V
Input/output supply voltage	2.5 V
Operating temperature	27°C
Simulation time length	100 ns

Voltage vs. time diagram is given in Fig. 6 where time scale is 100 ns and step is 0.1 ps. We can see in simulation graphs, the time delays and bus values. Voltage/current diagram is given in Fig. 7 where scale is 1 mA, time scale is 100 ns and step is 0.1 ps. We can see in the simulation graphs, the delays and bus values.

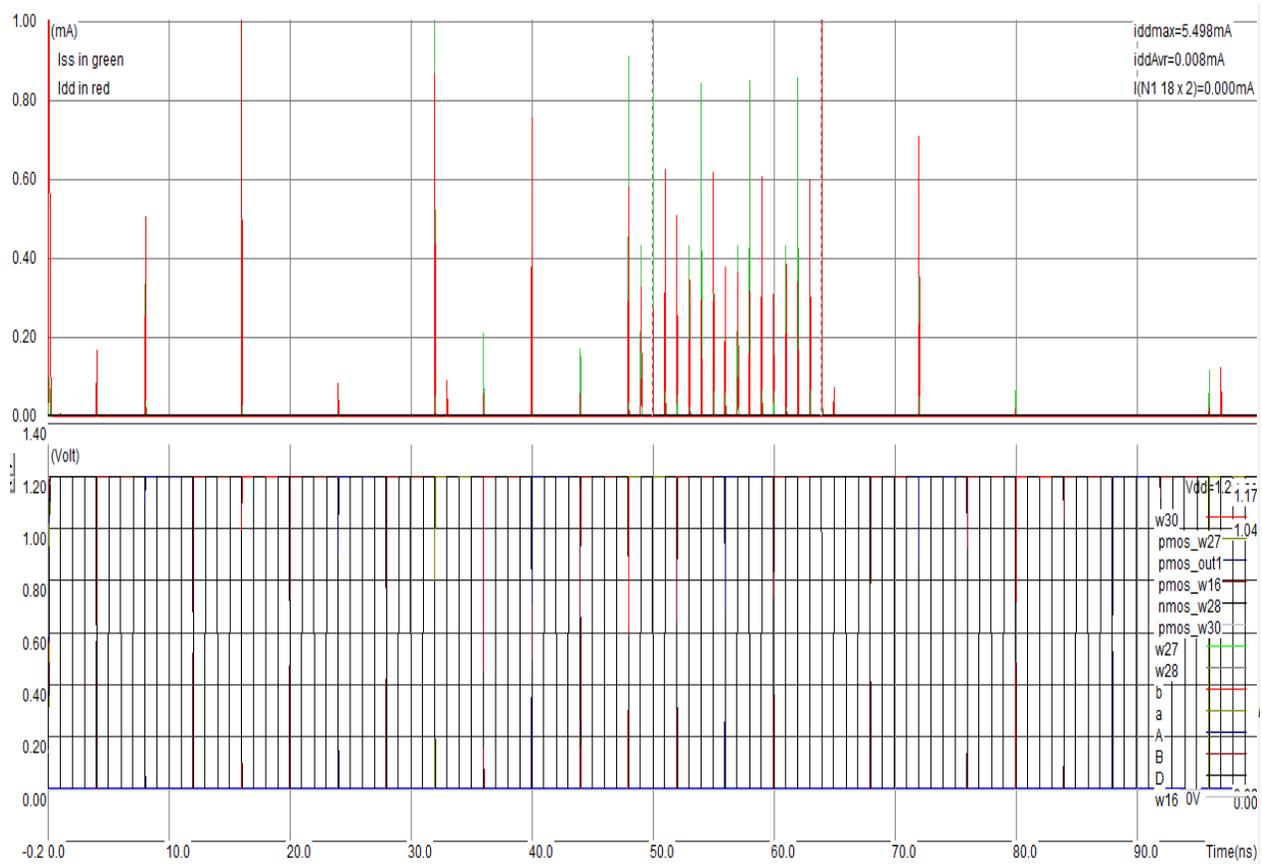
Table 3 shows the time taken by different inputs to reach to the high and low voltage levels of binary values due to change of signals/data. After the simulation, various data has been found and these are presented in Table 4. It indicates low power consumption of the designed circuit.



**Figure 6:** Voltage vs. time simulation graph

**Table 3:** Data analysis of voltage vs. time

Voltage (V)	Time (ns)				
	$S_1$	$S_0$	$D_3$	$D_1$	$D_0$
3.3	31.96	15.90	7.82	4	1
0.0	63.56	31.96	15.90	8	2
3.3	95.89	47.77	23.80	12	3
0.0	127.64	64.34	31.88	16	4
3.3	159.88	80.07	39.87	20	5
0.0	191.7	96.05	47.83	24	6



**Figure 7:** Voltage and current vs. time simulation graphs

**Table 4:** Current and voltage data obtained from simulation

$I_{dd,max}$ (mA)	$I_{dd,avg}$ (mA)	$V_{dd}$ (V)	$P_D$ ( $\mu$ W)	PMOS (W30) (V)	PMOS (W27) (V)
5.498	0.008	1.2	9.238	1.17	1.04

## V. Conclusions and Future Scopes

In this paper, transmission logic gate based multiplexer circuit has been designed, simulated, analyzed and tested. The post layout simulations of a 4:1 multiplexer circuit design process and simulation designs are presented at 90 nm CMOS technology node. From our simulation results, we have observed that the transmission gate based design of the multiplexer circuit operates very fast. The propagation delay in transmission gate logic is only 83 ps. The designed 4:1 multiplexer circuit shows better performance.

As future scopes of the work, the 4:1 multiplexer circuit can be developed using different types of MOSFETs and at different technology nodes. Besides, the performances parameters may be compared and analyzed for

various technology nodes. Eventually, its reverse logic circuit that is a de-multiplexer circuit can be designed using CMOS based technology. Not only that we can optimize the proposed architecture in term of area, power consumption and dissipation, speed of operation and so on. At present, Quantum dot Cellular Automata (QCA) based logic circuit design is receiving popularity in the nano-scaled regime. Therefore, there is a scope of designing the 4:1 multiplexer using QCA.

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