Design And Analysis Of 1:4 Bit Demultiplexer Using CMOS Technology

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Abstract— Research into combinational circuits is vital now since low power and low energy consumption are major concerns in consumer devices. A demultiplexer, also known as a data distributor, is a crucial component of digital circuits because it allows for the distribution of data from a single input to multiple outputs. Due to the widespread adoption of demultiplexers as a common component of digital combinational logic circuits/systems in integrated circuits, it is crucial to design or refine a demultiplexer architecture that can function efficiently while simultaneously conserving power. In this study, the performance of several demultiplexer architectures utilizing complementary metal oxide semiconductor (CMOS) logic is studied. Through the use of DSch and Microwind CAD tools, this research designs and analyzes a transistor-level CMOS logic-based 1:4 demultiplexer.

Keywords— CMOS, Demultiplexer, DSch, Microwind, MOSFET, Transistor.

I. INTRODUCTION

Traditional transistors present significant challenges for the semiconductor industry. A common example is leakage current. Off-state current (Ioff), which flows through the channel of the transistor while the device is idle and no voltage is applied on the gate, has constantly increased due to the shrinking size of transistors [1]. This effect of CMOS scaling could be mitigated, however, by modifying the device topology [2][3]. Therefore, power is lost as heat, making the CPU hot enough that the cooling fan must run longer to dissipate the excess heat.

With the rise of mobile devices like smartphones and laptops, power dissipation has emerged as a critical issue in VLSI design. Given that batteries can only provide intermittent power, electronics are continually getting smaller as designers strive to create circuits that use the least amount of power possible. While the CMOS circuit uses very little power when at rest, it can quickly become a major issue due to its high dynamic power consumption. Even though the pull-up network only made use of energy at the output load, it consumed fifty percent of the total available power. While the electricity is being switched on or off, any energy that has been stored in the load being discharged is dissipated to ground via a pull down network. This means that for a single cycle of operation, the CMOS circuit will dissipate its full amount of power.

A demultiplexer, or demux, is a piece of equipment that takes a single input signal (analog or digital) and converts it into a string of multiple outputs. If there are 2^n outputs, then there must be n select lines for the demultiplexer to route the binary data from the input line to the desired output [4]. Demultiplexers are widely used to increase the quantity of data that can be sent over a network in a specified amount of time and capacity [5][6][7]. The demultiplexer is a crucial part of any digital system. It has wide application in architectures with complex data paths [8][9]. Since the early 1980s, CMOS technology has been utilized to construct high-speed, low-size logic circuits. Dissipation in the PMOS network accounts for half of the power lost in a CMOS logic circuit, and the discharge of the output load capacitor during switching events is responsible for the remaining half [11]. Unfortunately, only about half of the energy that is drawn from the wall socket is really put to use. Logic circuits are increasingly being designed using CMOS technology at different nodes [12][13][14] due to the benefits it provides in terms of reduced surface area, increased energy efficiency, and decreased power dissipation.

The dissipation of power during computation has been determined to be fundamentally related to the amount of work being done on the computer. Without any data loss, the logic for processing could be implemented, and eventually their energy needs could be lowered to zero. All computations must be performed

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in a reversible manner for this to be possible. How much power is lost is determined by the typical decrease in voltage that a charge must experience before reaching the load capacitance. Lowering power consumption in digital designs is possible through the use of lower voltage steps or increments [15][16][17]. Adiabatic switching refers to the use of the least amount of energy possible during the charge transfer phase. Although standard CMOS logic uses a constant voltage source to energize its components, adiabatic logic uses a constant current source to accomplish so. It receives its electricity from a source that generates either trapezoidal or sinusoidal waves. Supply voltage, switching frequency, and node capacitance values are all modifiable parameters that influence power dissipation. Many digital circuits have seen an increase in performance when these values were reduced or the topologies were changed.

A variety of studies have been conducted to develop the 1:4 demultiplexer [20-30]. Rehman et al. designed a 1:4 demultiplexer consumes a total of 77 mW of power while using a 1 V supply voltage [20]. The 1:4 demultiplexer that B.-G. Kim et al. developed has a total power consumption of 210 milliwatts and operates off of a supply voltage of 1.2 volts [25]. P. Min et al. created a 1:4 demultiplexer that operates at a speed of 12 Gb/s with a power supply voltage of 1.8 V and a power consumption of 56 mW [27].

This paper's purpose is to describe the design and analysis of a CMOS-based digital logic circuit for a 1:4 demultiplexer and to provide insight into the circuit's performance characteristics.

The remainder of this article will consist of a review of relevant literature, followed by the derivation of the theoretical development of the work, a description of the design, and a simulation of our circuit, followed by the presentation of the results and a discussion of relevant aspects of the simulation results. Finally, we will offer some suggestions for future research.

II. DEMULTIPLEXER

Demultiplexer is a circuit in which n select lines select one of 2^n input lines and selected line goes to output. When developing control systems or dynamic circuits, a demultiplexer is a crucial part [18]. Demultiplexers are used to increase data throughput within a certain time and bandwidth constraint. For the purpose of data distribution, a Demultiplexer may be referred to as [19]. The block diagram of the designed 1:4 demultiplexer is depicted in Fig. 1. Fig. 2 illustrates the circuit diagram for the 1:4 demultiplexer.

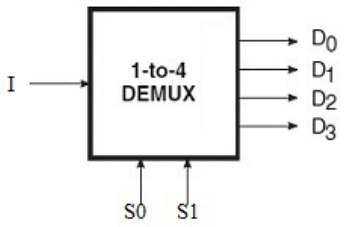

Figure 1: Block diagram of 1:4 Demultiplexer.

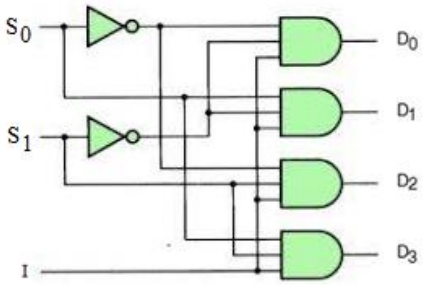

Figure 2: Circuit diagram of 1:4 Demultiplexer.

A 1:4 demultiplexer comprises an input line as *I:* two select lines as S_0 and S_1 and four data output lines as D_0, D_1, D_2 and D_3. When deciding which of the four output lines (D_0–D_3) should be connected to the input line, selector lines S_0 and S_1 consult Table 1. To describe this in its simplest form, a Boolean equation can be used. The following equation provides the Boolean expression (D_0 through D_3) for the 1:4 demultiplexer with data input lines I and data selection lines S_0 and S_1.

$$D_0 = \overline{S_1}\,\overline{S_0}I$$
$$D_1 = \overline{S_1}S_0I$$
$$D_2 = S_1\overline{S_0}I$$
$$D_3 = S_1S_0I$$

Input	Select Lines	Output Lines
I	S_1 S_0	D_0 D_1 D_2 D_3
I	0 0	1 0 0 0
I	0 1	0 1 0 0
I	1 0	0 0 1 0
I	1 1	0 0 0 1

Table 1: Truth Table of 1:4 demultiplexer.

A. *Different Logic Styles*

Logic style can be defined as how transistors are used to realize logic function. Speed, size, power dissipation and wiring complication are the features which rely on which logic style is used and they are vary noticeably from one logic style to other logic styles and therefore,

for circuit concert selection of appropriate logic style is very helpful.

1) DPTL (Dual Pass Transistor Logic)

Dual Pass Transistor Logic is the most potent structure in CMOS technology (DPTL). To compensate for input signal-swing variations, DPTL buffers are able to provide CMOS-typical levels.

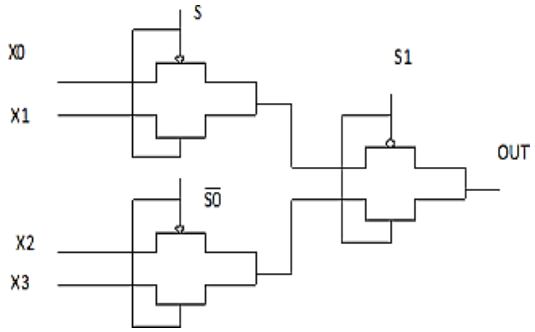

Figure 3: DPTL base 1:4 Demultiplexer.

The PMOS and NMOS transistors of a DPTL are coupled in parallel to form the basic structure. Through the swapping of NMOS and PMOS, VDD and GND, a dual logic function is formed in DPTL. A DPTL demultiplexer with a base 1:4 conversion is shown in Fig. 3. The diagram in fig. 3 illustrates a DPTL base 1:4 demultiplexer.

2) Positive Feedback Adiabatic Logic (PFAL) Based 1:4 Demultiplexer

The PFAL approach is a dual-rail partial adiabatic method. A simplified version of the circuit is shown in Fig. 4. For PFAL to work, adiabatic amplification is essential. Inverter pairs that are cross-coupled are what make up the PFAL latch. As an alternative to the conventional clock used to energize the logic networks, it makes use of a power clock.

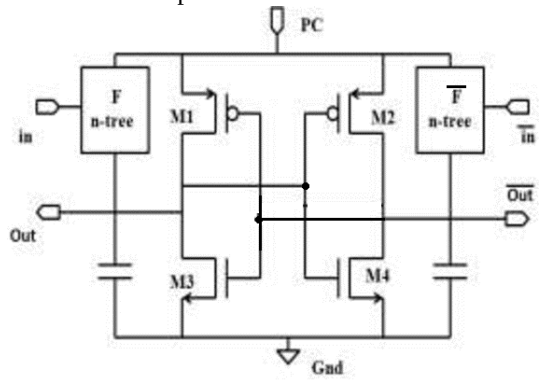

Figure 4: PFAL logic circuit.

A time-varying signal is employed to activate the circuit elements and timing control, and no additional dc power is required. A low-resistance connection is established between the relevant input and the power clock via one of the logic blocks. To prevent the power clock from reaching the other concerned output, the other logic network features a very high resistance link. The other one of the two outputs is connected to ground, while the first one is brought up to the power clock.

Attenuation of the signal at the outputs is kept to a minimum by PFAL. In parallel with PMOS, the F and $\bar{F}$ tree logic blocks provide full-swing performance reminiscent of transmission-gate technology. The logic inputs are taken care of by the F and $\bar{F}$ functions. In contrast to alternative adiabatic circuits, the resistance provided here is lower. Recovering the power supplied by the power clock is optimized by PFAL's usage of the four-phase clocking rule.

3) Cascade Voltage Switch Logic Based 1:4 Demultiplexer

Low-power consumption is a primary design goal of the CMOS-type logic family known as Cascade Voltage Switch Logic (CVSL). The logic was implemented with NMOS transistors, which can handle both true and complementary input signals, and two P-channel transistors were added to the design to make sure one of the outputs was always pulled to the highest possible level. This class of logic is sometimes referred to as Differential Cascade Voltage Switch Logic (DCVS or DCVSL). The CVSL logic circuit is displayed in fig. 5.

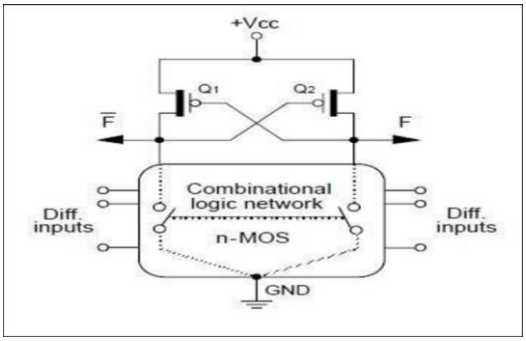

Figure 5: CVSL logic circuit.

4) CMOS Transmission Gate Logic Based 1:4 Demultiplexer

Transmission gates can be used to isolate many signals with minimal board area investment and with only a slight loss in the properties of those crucial signals, all while serving their intended purpose and operating in a straightforward manner. Signal levels can be blocked or passed through a transmission gate from the input to the output. A PMOS transistor and an NMOS transistor are linked together in parallel to provide the solid-state switch. To ensure that both

transistors are either on or off, the control gates are biased in a complimentary fashion.

The gate of the n-channel MOSFET is shown in fig. 6 to be at a negative supply voltage potential when the control input is logic zero. The inverter is responsible for connecting the p-channel MOSFET's gate terminal to the power supply's positive end. The gate-source voltage of n-channel MOSFETs is always negative, while that of p-channel MOSFETs is always positive, within the allowable voltage range, regardless of which switching terminal of the transmission gate (A or B) the voltage is applied to. As a result, the transmission gate is disabled and neither of the two transistors conducts.

Any time the logic one is present at the control input, the gate terminal of the n-channel MOSFETs will be connected to the power supply's positive rail. As a result of the inverter, the gate terminal of the p-channel MOSFETs is now connected to a negative supply voltage. The transistors begin operation with a voltage differential between the gate terminal and one of the conducts (the drain or the source), as the substrate terminal is not linked to the source terminal. Therefore, the layout is not preferred for less advanced technologies.

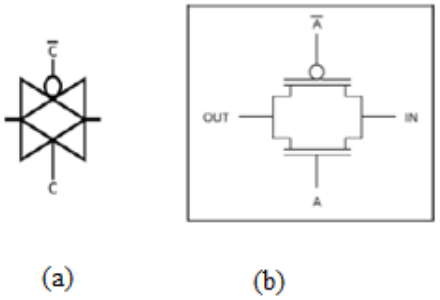

Figure 6: (a) Symbol of transmission gate, (b) Schematic representation of transmission gate.

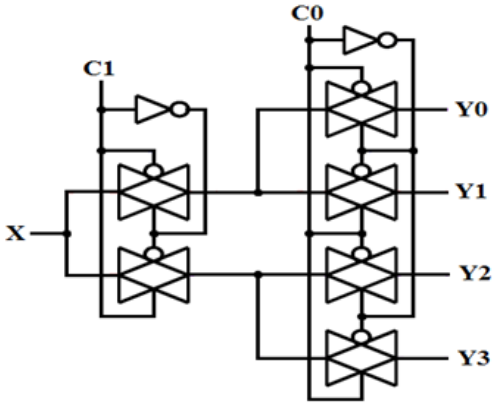

Figure 7: TGL base 1:4 Demultiplexer.

The focus of this research was the creation of a 1:4 demultiplexer using CMOS technology. The proposed design uses only 12 transistors, drastically reducing power usage while taking up as little room as possible. Figure 7 is a high-level schematic depicting how a 1:4 demultiplexer is built using transistors. The selection bits (C1 and C0) and the data bit (X) make up the demultiplexer circuit. There are four possible destinations for the data X, and which one receives it depends on the values of the selection bits.

III. Simulation Results and Discussions

Two programs have been used for the design, simulation, and analysis that has been carried out here. The layout is extracted from the circuit schematic that was designed in DSch software at a 90 nm CMOS process. The Verilog file was created after running this design file via a simulation. Microwind software is then used to simulate the layout diagram in order to evaluate the designed circuit's performance.

Using the proteus software, fig.8 displays the design for the proposed task.

Fig.9 depicts the intended circuit of the 1:4 demultiplexer created in the DSch program.

Using the 90 nm CMOS technology in Microwind, fig. 10 demonstrates the layout of a 1:4 demultiplexer circuit retrieved from DSch.

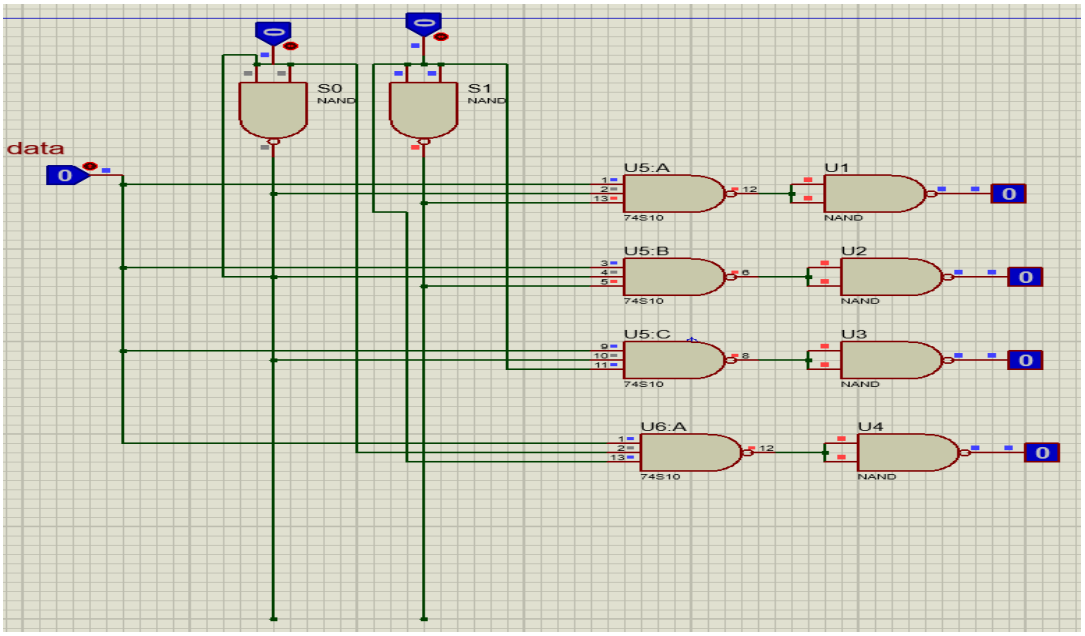

Figure 8: Design schematic of a 1:4 demultiplexer using proteus software.

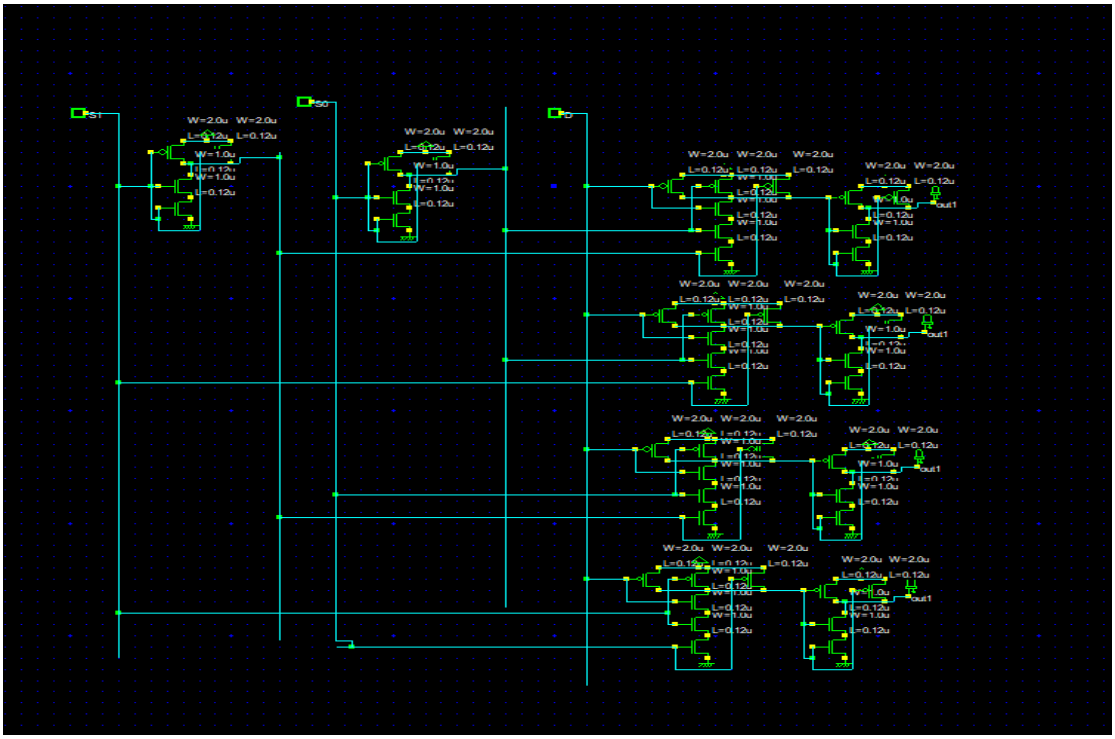

Figure 9: Layout Diagram of a 1:4 demultiplexer using CMOS technique in DSch

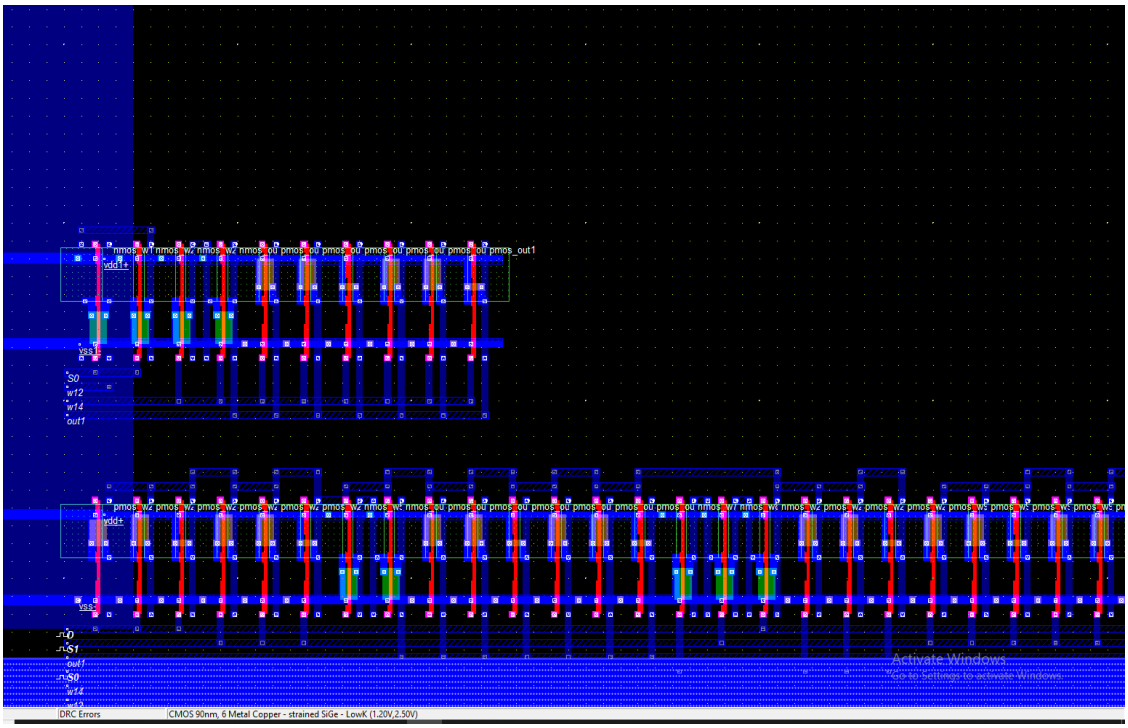

Figure 10: Layout diagram of a 1:4 demultiplexer using CMOS in Microwind

In this study, we present a CMOS implementation of a digital 1:4 demultiplexer that consumes very little power. In Table 2 you'll find the simulation settings for the implemented circuit.

Table 2: Simulation parameter values

Supply voltage	1.2 V
Input/output supply voltage	2.5 V
Operating temperature	27°C
Simulation time length	100 ns

As shown in fig.11, voltage is plotted against time with a 100 ns time scale and a 0.1 ps step. The simulation results are visualized as graphs showing the time lags and bus values. As shown in fig.12, a voltage/current diagram is provided with a 1 mA scale, 100 ns time scale, and 0.1 ps step. Graphical representations of the simulation outcomes, including delay times and bus values, are presented.

Fig. 13 displays the current and voltage values that are obtained through simulation.

Time required for various inputs to transition between the high and low voltage levels of binary values owing to a change in signals/data is shown in Table 3. Table 4 displays the results of several measurements taken after the simulation was run. It's a promising indicator when the designed circuit has a low power consumption.

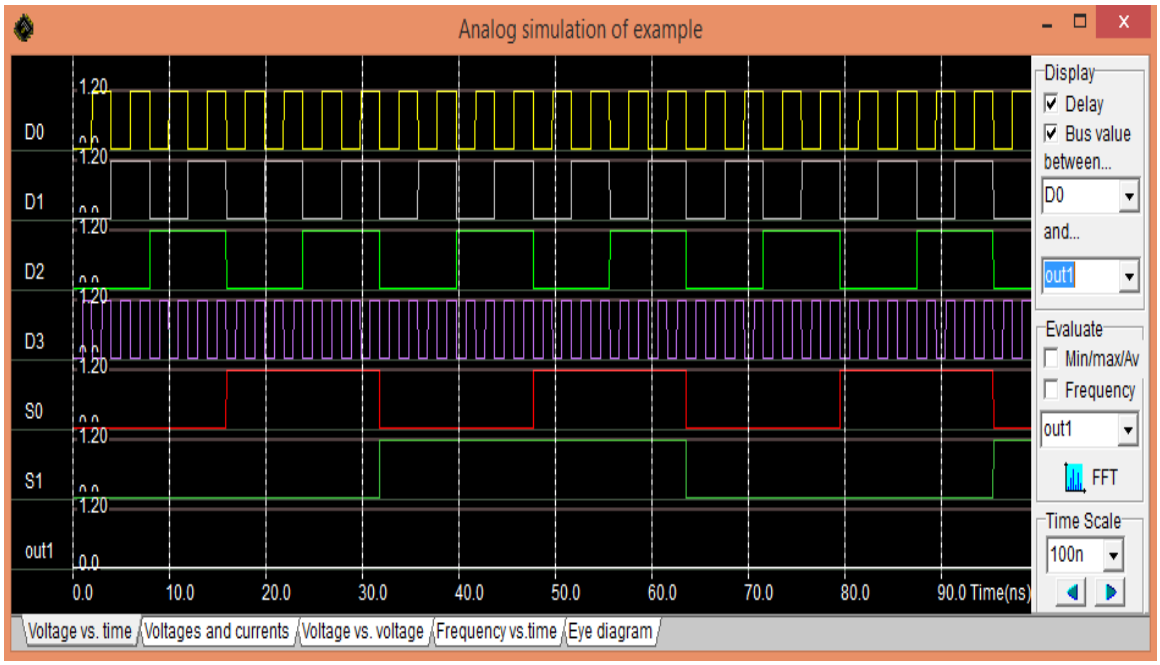

Figure 11: Voltage vs. time simulation graph

Table 3: Data analysis of voltage vs. time

Voltage (V)	Time (ns)				
	S1	*S0*	*D3*	*D1*	*D0*
3.3	31.96	15.90	7.82	4	1
0.0	63.56	31.96	15.90	8	2
3.3	95.89	47.77	23.80	12	3
0.0	127.64	64.34	31.88	16	4
3.3	159.88	80.07	39.87	20	5
0.0	191.7	96.05	47.83	24	6

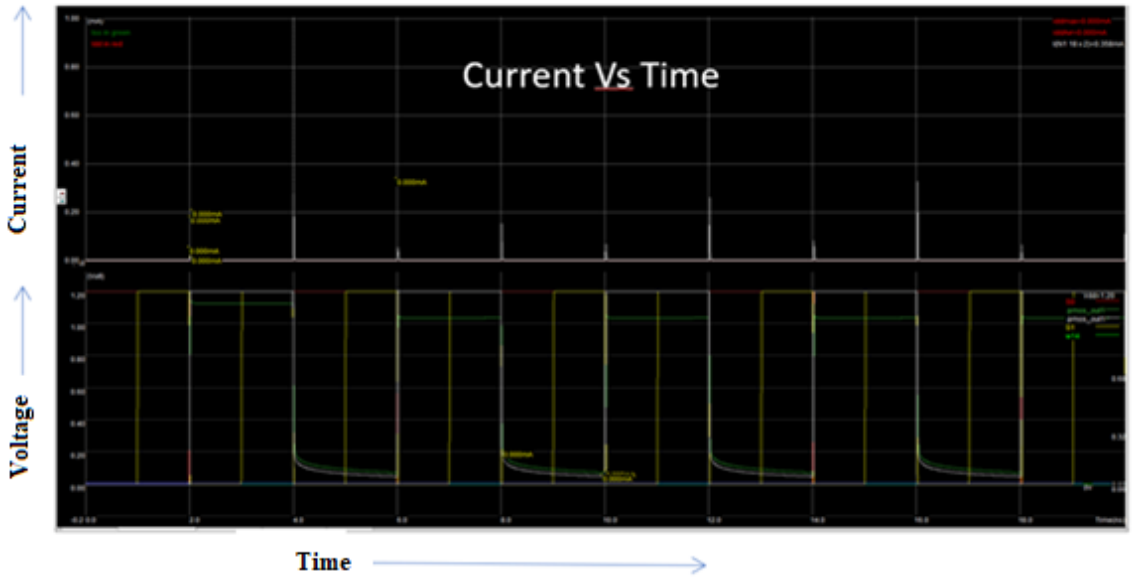

Figure 12: Voltage and Current vs Time.

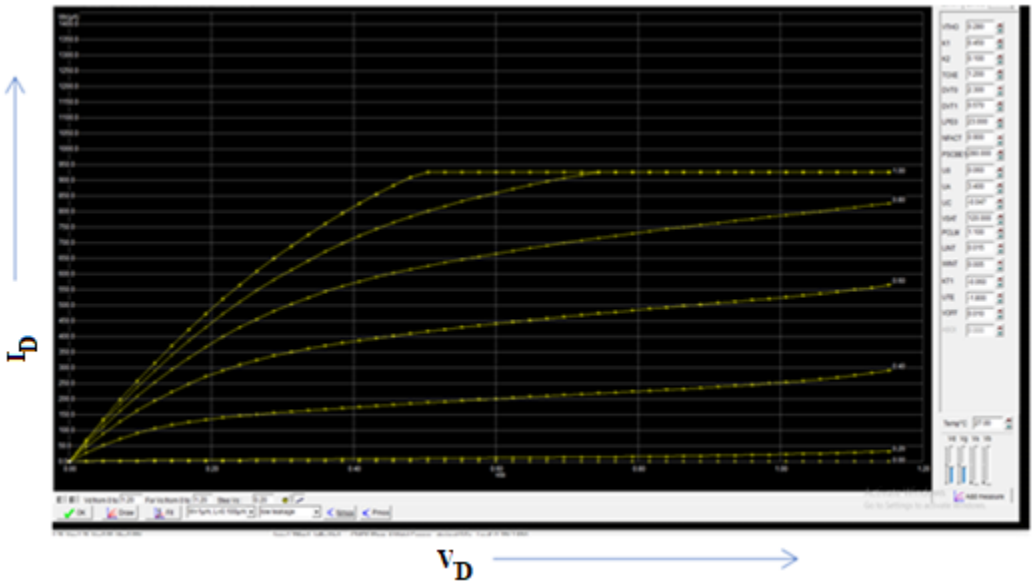

Figure 13: I_D vs V_D of MOSFET.

Table 3: Data obtained from simulation

Sr.No	Properties	1:4 DE-MUX using gate
1	Rise delay	19 pS
2	Fall delay	5 pS
3	No of transistors	36
4	Power consumption	77.561 µW

IV. CONCLUSIONS AND FUTURE SCOPES

Demultiplexer circuits based on transmission logic gates are proposed, with a primary emphasis on reducing power consumption. The simulation designs and post-layout simulations for a 1:4 demultiplexer circuit in 90 nm CMOS technology node are shown in this research. Our simulation findings reveal that the transmission gate based design of the demultiplexer circuit is the most efficient in speed and uses the least amount of power while simultaneously decreasing the delay parameter. Transmission gate logic has a very short propagation latency of 83 ps.

Future work scopes for the 1:4 demultiplexer circuit may include investigating its use of alternative MOSFET types and technology nodes. There is the possibility of designing the 1:4 demultiplexer by using the silvico software. Presently, in the nano-scaled regime, interest is growing in logic circuit design based on Quantum dot Cellular Automata (QCA). As a result, QCA can be used in the design of the 1:4 demultiplexer.

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