A REVIEW ON THE PROGRESS OF HIGH PERFORMANCE CMOS VOLTAGE BUFFER

Nahid Akhter Jahan and Md. Mamun Bin Ibne Reaz

***Abstract*—** Abstract: In general, high DC gain and high unity gain frequency become as crucial parameters and much interest in the state of art in designing low power and low voltage application of analog IC circuits. In this modern deep submicron Complementary Metal Oxide Semiconductor (CMOS) technology, one of most versatile and indispensable blocks which promises those advantages is a voltage buffer. Its architecture plays essential role in driving low impedance loads at high speed with minimal power consumption through the replication of its input signal to the output regardless of connected load and environmental conditions of the output. This paper presents a review of several various commonly encountered topologies and architectures of CMOS voltage buffer and relationship between these topologies with several parameters, to understand the progress of high performance CMOS voltage buffer. We surmise that from this review and discussion, researcher will get benefit in choosing the most suitable topology of CMOS voltage buffer for desired advantages.

***Keywords*—**Voltage buffer; CMOS; low voltage; linearity; harmonic distortion; bandwidth; slew rate

I. INTRODUCTION

The study of operational amplifier (op-amp) as a voltage buffer using CMOS technology has become a great interest among analog designers for past few years. CMOS technology is preferable compared to other existing technologies such as Bipolar and BiCMOS mainly due to its economical choice. It offers a wide range of advantages such as low power dissipation, longer rise and fall time, shorter propagation delay, less complex circuit, higher noise immunity and lower system level cost.

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In very large scale integration (VLSI) CMOS based system, voltage buffer has been widely used in designing low voltage and low power devices such as analogue multipliers implemented in mixers, filters, detectors, modulator and soft computing application [1].
It is also one of the key modules in A/D converters, comparators, current-conveyors, low dropout regulator, sensors, operational transconductance amplifier (OTA), wide tuning filter range application and also in wireless communication [2-10]. One of the main features to achieve the success of these systems is the capability of voltage buffer in driving large capacitive loads and/ or resistive loads while maximizing energy transfer in between the circuits of the system.
During the past three decades, several topologies of CMOS voltage buffer have been reported and dominated the semiconductor industry. Despite of these topologies, its performances are greatly influenced by several stringent parameters, which imposes great contribution to the high performance of CMOS voltage buffer in the VLSI era. For example, in the world of wireless communication, it becomes compulsory requirements for portable electronic devices to be operated in a low voltage supply, low power consumption and low distortion as demanded by the market nowadays. Strictly speaking, depending upon the requirements, the topology should be wisely selected. Therefore, in this paper we intended to study and analyze more than a few various commonly encountered topologies and architectures of CMOS voltage buffer and the correlation between these topologies with several pertinent parameters, so that we can realize the contribution and development of the typical high performance CMOS voltage buffer in IC circuits so far.

II. VOLTAGE BUFFER PRINCIPLE

A non-inverting amplifier (or also known as voltage amplifier) configuration shown in Figure 1 is the basic principle in designing the voltage buffer which has large input resistance (R_1) and small output resistance (R_2). For linear voltage amplifier, the output signal (V_o) is the amplification factor, known as the amplifier gain (A_v) multiplied by the value of the input signal (V_i); $V_o = A_v * V_i$. Thus, bigger value of A_v will better the voltage amplifier.

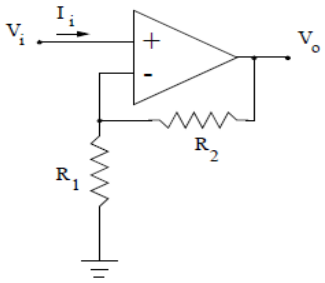

Fig. 1. Non-inverting amplifier.

Through the equation; I = V/ R, if R_1 is large enough (or infinity), it is equivalent to ∞ (open circuit) and the value of I will be very small (or nearly to zero). If R_2 is very small (or zero), the value of I will be very huge and R_2 may then be removed.

In addition, if A_v of the voltage amplifier is designed to be 1 or unity, there will be no amplification at the output terminal i.e the output signal is connected back to the input and the output voltage is same value as the input voltage. Thus, the voltage amplifier is regarded as a buffer since no signal amplification and so is as 'isolator' between two circuits in order to prevent the operation of one circuit affecting the operation of the other. This kind of voltage amplifier with gain 1 is known as voltage buffer, voltage buffer amplifier, voltage follower, source follower, unity gain amplifier, buffer amplifier or isolation amplifier [11] and is presented in Figure 2 [10].

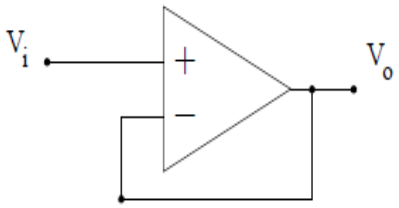

Fig. 2. Voltage buffer [10].

The main purpose of the voltage buffer having large input resistance with a very small current and small output resistance with a huge current is to reduce any disturbances and high use of power source in powering any load. With small output resistance, the circuit will drive the load as if the source comes from the original voltage with a minimal disturbance in the original circuit. It will then contribute to reduction in power consumption in the source, distortion from overloading, crosstalk and interference due to electromagnetic [12].

In a complex device such as current feedback op-amps and various types of current conveyers, voltage buffer will be one of the basic cells. However, voltage buffer can also be as a stand-alone device [13]. In the field of analog and mixed signal CMOS circuit design, voltage buffer is very important and essential device where a weak signal needs to be delivered to a large capacitive load [14]-[15] or large resistive load [11] at high speed. In VLSI CMOS systems, a large capacitive load will give a very significant impact due the deep submicron CMOS technology. This is because the overall bandwidth of the system will have a limitation due to the loading effect by large capacitive load. Thus, a well design or high performance voltage buffer using CMOS process is needed to overcome certain drawbacks due to the large capacitive load.

III. VOLTAGE BUFFER TOPOLOGIES AND ARCHITECTURES

A. Basic CMOS voltage buffer (VB)

Figure 3 presents a basic schematic diagram of CMOS voltage buffer [16]. The input at the gate will determine the value at the output (i.e source terminal). Thus, M1 will be acting as the follower to the output current. If a resistor, r_o (Z_L) is connected in between source and supply at drain-voltage, it can be calculated as 1/ gain coefficient, g_m of M1 [14].

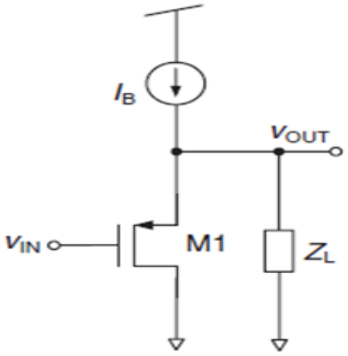

Fig. 3. Basic schematic diagram of CMOS voltage buffer [16].

However, by applying a small value r_o, it is no guarantee the same value of current will flow through the source [12]. Thus, this kind of design is unsuitable for low voltage application due to non-linearity [12], limitation in the output swing due to the associated DC level shift [14] and difficult to achieve a unity gain [12]. Besides that, by placing a small value of r_o and increasing the value of g_m will cause an increasing in the value of I_D. Indirectly, the ratio of W/L will be larger and the size of transistor will be bigger which then will become

unsuitable for submicron technologies. Besides, it will also increase the power dissipation [12].

B. Flipped voltage follower (FVF)

Figure 4 presents a design of voltage follower with shunt feedback or local feedback which is also known as flipped voltage follower, FVF [16]. The purpose of local feedback is either increasing or decreasing signals swing and impedance levels at certain node. FVF is more suitable for class-AB implementation [17]-[18].

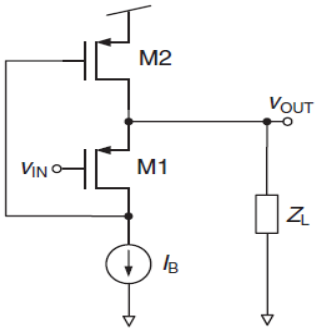

Fig. 4. Flipped voltage follower [16].

In FVF, M2 will provide variation in the output current while keeping a constant current for M1 which is equal to I_B. So, $V_{GS}M_1$ will be held constant and it is possible to get a unity gain [17]. Thus, it is suitable for low power and low voltage application [1]. However, even though this kind of topology may improve the linearity of the FVF, in deep submicron technology, it will limit the output swing [12], [19].

C. Bulk driven flipped voltage follower (BFVF)

Figure 5 represents a design of bulk driven flipped voltage follower, BFVF [19] which will preserve the advantages of FVF but with higher slew rate and output swing.

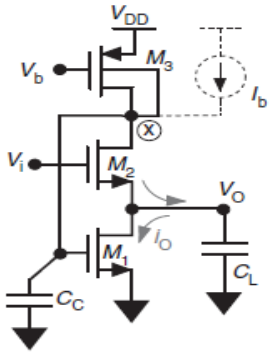

Fig. 5. Bulk driven flipped voltage follower [19].

An additional transistor, M_3 is attached to node 'x' acting as an adaptable current source. The value of V_{GSM3} is fixed by V_b and the voltages at M_1 and M_3 are controlled by the voltage at node 'x'. V_{GSM2} will increase if V_i increases. However voltage at node 'x' will reduce and M_1 will turn off. Thus, it will increase V_{BM3} and allow high current in M_3. Since M_1 turns off, V_o will follow V_i.

D. Class-A voltage follower

Figure 6 presents a design of class-A voltage follower [20]-[21]. As being stated earlier, the voltage buffer will have high input impedance and relatively low output impedance to ensure a large values of I_{CL}.

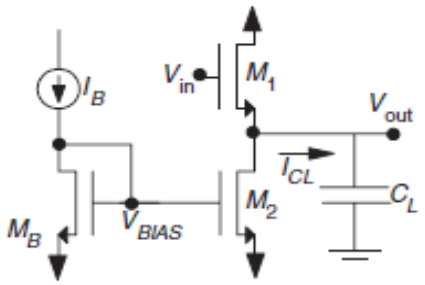

Fig. 6. Class-A voltage follower [20]-[21].

Through the given equation;

$$dV_{out}/dt = [\tfrac{1}{2}\{K_n * (W_{M1}/L_{M1})[V_{in}-V_{out}-V_{th}]\}^2 - I_{CL}]/C_L \quad (1)$$

$$BW = g_{M1}/(2\pi C_L) \quad (2)$$

where K_n is the NMOS intrinsic transconductance, V_{th} is the threshold voltage and BW is the bandwidth, the rate of the output voltage can be calculated. The current through M_1 will increase due to a large voltage difference between V_{in} and V_{out}, thus C_L will be charging. However, the current flow out of C_L is only provided by I_{CL} when V_{in} decreases. Thus, the maximum rate at which the output voltage can change is only $-I_{CL}/C_L$ since I_{CL} is constant.

If the circuit is designed for a large capacitive load, I_{CL} can be set as large enough to ensure a high slew rate for the output. However, this will cause large power consumption and reduction in output voltage swing [21].

E. Class-AB voltage follower

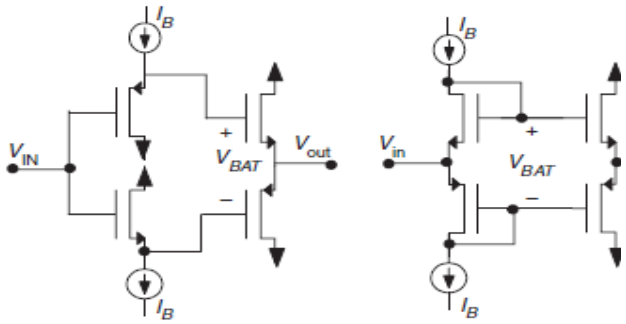

Fig. 7. Class-AB voltage follower [20].

Figure 7 shows two common designs of class-AB voltage follower [20]. In class-AB voltage follower, the common collector or drain are connected with complementary transistors. By having these designs, larger dynamic currents can be provided than class-A voltage follower. However, the main drawback is, it will increase the voltage supply; $V_{dd} = 2\ (V_{GS} + V_{DSsat})$ [20] where it requires double values for gate to sources voltage supply [2]. Besides it has limited output swing [2] and linearity problem. Even though class-AB follower is known as preferable device in current handling capabilities due to a very small quiescent current [2], suitable buffer to drive high capacitive load and also have almost similar bandwidth, output impedance and distortion as class-A voltage follower but most class-AB follower will have more power dissipation due to its complex circuit [20].

F. Transconductance amplifier based voltage follower (TVF)

Due to several drawbacks for a large capacitive load, it is common to design a voltage buffer having a transconductance amplifier connected in negative feedback as presented in Figure 8 [22].

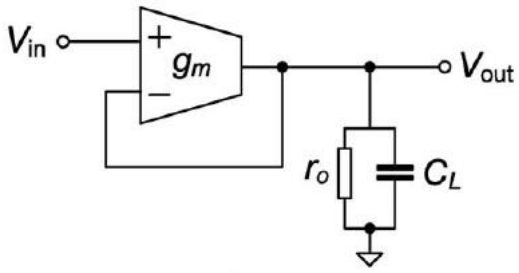

Fig. 8. Transconductance amplifier based voltage follower [22].

Generally, the main function of transconductance amplifier is merely similar to the voltage amplifier except that transconductance amplifier will amplify an output current with the input voltage i.e. is also be known as 'voltage to current' converter.

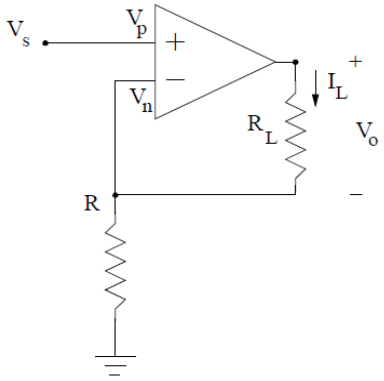

Fig. 9. Transconductance amplifier.

Thus, by using the concept of voltage amplifier where $A_v = 1$, $R_1 = \infty$ and $R_L = 0$, the transconductance amplifier is acted as voltage buffer which able to drive large capacitive load.

By referring to Figure 8, C_L is represented as the load capacitor and r_o is the output resistance of the g_m circuit. In order, to quickly charge (or discharge) C_L, g_m circuit should have a high output current drive capability so that V_{out} will follow the V_{in} value. This kind of design is widely used in analog testing and signal monitoring, liquid crystal display drivers and low-drop-out regulator. Another design of transconductance amplifier based voltage follower can be seen in Figure 10 and Figure 11, respectively [23].

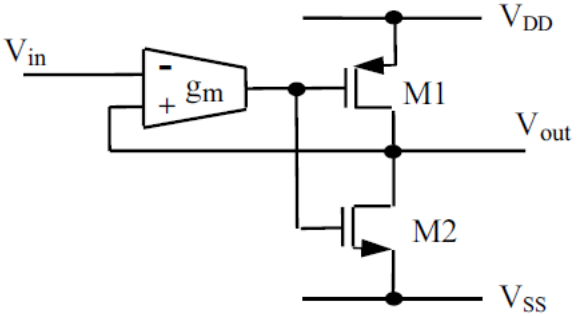

Fig. 10. Another design of transconductance amplifier based voltage follower [23].

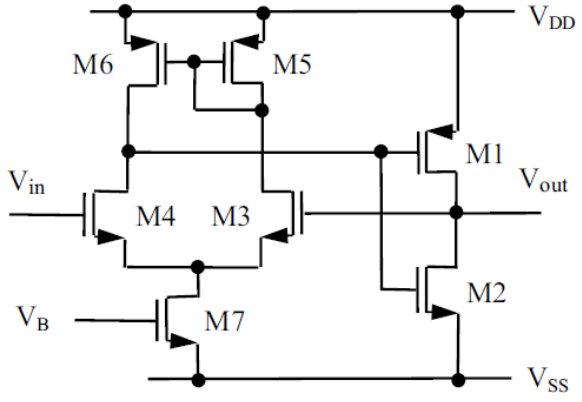

Fig. 11. CMOS circuit realizing the alternative design of Figure 10 [23].

The design consists of g_m circuit and a pair of complimentary CMOS inverter (M1 and M2) where g_m circuit is built of the M3-M7 transistors. The circuit is designed with gain 1 and a strong negative feedback to ensure a very high input impedance and low output impedance.

G. Super class-AB bulk driven operational transconductance amplifier (BD OTA)

Figure 12 presents a super class-AB BD OTA which is based on bulk flipped voltage follower for the bulk driven input stage (or known also as adaptive biasing) and a nonlinear current mirror [24]. The purpose of adopting adaptive biasing and current mirror is to improve the slew rate. The adaptive biasing composes of two cross coupled BFVFs and matched input differential pairs. By having the local feedback and enhanced transconductance, it improves the gain bandwidth. However, due to its complex circuit, it lead to slightly higher power dissipation.

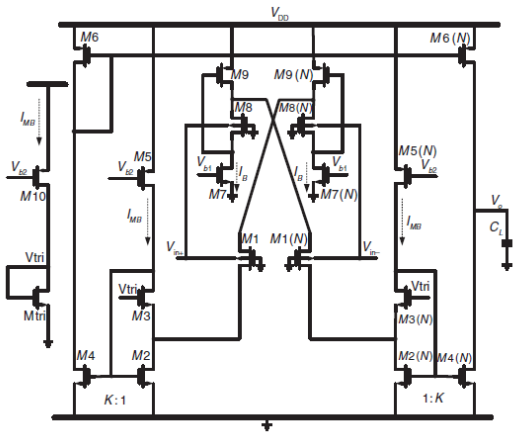

Fig. 12. Superclass-AB BD OTA [24].

A brief summary on advantages and limitations of the above topologies are shown in Table 1. Generally, the application of CMOS voltage buffer and its requirements will determine which topologies of voltage buffer will be selected because each design will have its own advantages and drawbacks.

As example, if the main concern in designing the voltage buffer is to increase the input signal voltage swing to its maximum value, then it is suggested to use buffer with local feedback, which is FVF. It is reported that by using FVF as the input stage to second generation current conveyer, besides voltage swing, it offers wider bandwidth, high speed and can be operated in a low voltage with low power consumption [17].

Class AB voltage follower is usually preferable for high power efficiency application [22] and portable electronics devices, as example battery. For the battery lifetime to be extended to its maximum duration, it is important to ensure low power consumption and high slew rate [25]. This becomes as major drawback for class A voltage follower because its maximum output current is limited by the bias current and hence will degrade settling time of the buffer [26]. Thus, class A buffer is unsuitable to drive portable electronics devices in wireless field that strongly requires a fast settling response.

For a large capacitive loads application, as example in LCD, TVF or BD OTA with smaller bulk transconductance mainly become one of suitable designs [14]. In LCD applications which requires high resolution, high quality and physically large panel size, slewing time normally dominates the settling time. The slew rate must be increased in order to reduce the settling time and this effect can be achieved through these two designs.

Besides the above CMOS voltage buffer topologies, there are few other CMOS voltage buffer topologies such as:

- super source voltage follower [25]-[27] where a transistor is introduced in the negative feedback to reduce the output resistance;
- bulk driven quasi-floating gate super source follower [14] where it includes a combination of quasi-floating gate technique and bulk driven technique;
- differential flipped voltage follower [22]; and
- pseudo voltage follower where the common source stage is used at the output to provide better voltage swing [28].

The discussion of the above selected topologies will be found in Section IV for better understanding. Section IV discusses several modifications of the above topologies in order to enhance the performance of CMOS voltage buffer.

Table 1. Summary on advantages and limitations of various topologies and architectures of CMOS voltage buffer.

	Topology of voltage buffer	Advantage	Limitation
A.	Basic CMOS voltage buffer (VB) [16]	• suitable for low resistance load	• non-linear [12] • limitation in output swing [14] • difficult to achieve a unity gain [12] • large ratio of W/L [12] • huge size of transistor [12] • high power dissipation [12]
B.	Flipped voltage follower (FVF) [16]	• unity gain [17] • low voltage [1] • low power consumption [1] • high linearity[16]	• limitation in output swing [12], [19]
C.	Bulk driven flipped voltage follower (BFVF) [19]	• high slew rate [19] • high output swing [19] • extension of operating voltage range	
D.	Class-A voltage follower [20]-[21]	• high input impedance [20]-[21] • low output impedance [20]-[21]	• unsuitable for large capacitive load [21] • high power consumption [21] • limitation in output swing [21] • high total harmonic distortion
E.	Class-AB voltage follower [20]	• small quiescent current [2] • suitable for large capacitive load [20] • wide bandwidth [29]	• high voltage [20] • limitation in output swing [2] • non-linear [2] • high power dissipation [20]
F.	Transconductance amplifier based voltage follower (TVF) [22]	• high input impedance [22] • low output impedance [22] • suitable for large capacitive load [20]	
G.	Super class AB bulk driven operational transconductance amplifier (BD OTA) [24]	• high slew rate [24] • high gain bandwidth [24]	• high power dissipation [24]

IV. PARAMETERS OF HIGH PERFORMANCE CMOS VOLTAGE BUFFER

Despites of having very high input impedance, very low output impedance and unity voltage gain, there are several other essential parameters that adversely affect the performance of CMOS voltage buffer. The parameters are low voltage supply, high linearity, low total harmonic distortion, wide bandwidth, high slew rate, low power consumption, high speed, large driving capability, wide input and output voltage swing, low noise performance and high power efficiency [30]-[39]. In this review article, the author will focus on selected crucial parameters which are unity voltage gain, low voltage supply, high linearity, low total harmonic distortion, wide bandwidth and high slew rate.

A. Unity voltage gain

[11] demonstrates a unity gain voltage buffer where the circuit capable to drive any resistive and capacitive loads. The circuit consists of one current mirror with a combination of three enhancement mode MOS transistors. Through this design, the output voltage is not affected to the threshold voltages and transconductance of the MOS transistors.

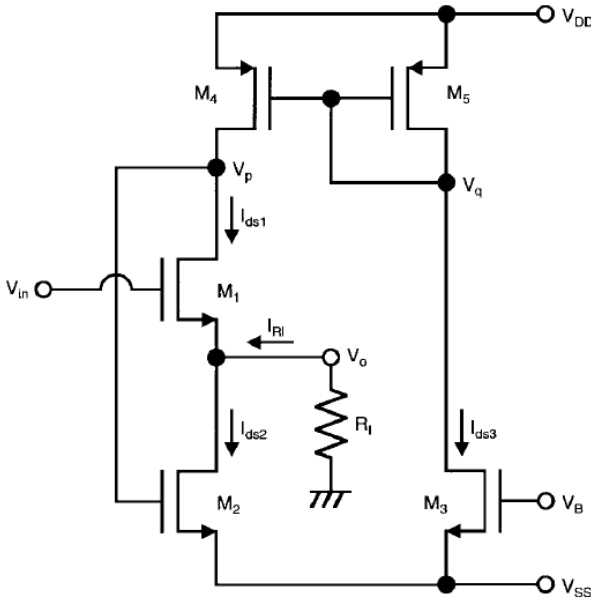

Fig. 13. Unity gain voltage buffer [11].

M_4 as the current source is controlled by the bias voltage (V_B). When M_1 and M_3 are operated in the saturation region, the drain-to-source current of M_4 (I_{ds1}) is equal to I_{ds3} through the current mirror (M_4 and M_5) which will then cause the gate-to-source voltage of M_1 (V_{gs1}) is equal to V_{gs3}. Thus, the voltage output (V_o) is determined by the input voltage (V_{in}) and V_B which is insensitive to the load.

In the saturation region, since the back gate of M_1 is connected to the source of M_1, the body effect can be neglected. The gain value (A_v) will depend on transconductance of M_1 and M_2 (g_{m1} and g_{m2}), drain conductance of M_1 and M_2 (g_{d1} and g_{d2}), output conductance of current mirror (g_{cm}) and conductance of R1 (g_{R1}). Through this equation,

$$A_v \simeq \frac{1}{1 + g_{Rl}\dfrac{g_{d1} + g_{cm}}{g_{m1}g_{m2}}}$$

$$\simeq 1 - g_{Rl}\frac{g_{d1}+g_{cm}}{g_{m1}g_{m2}} \quad (3)$$

the value of g_{d1} and g_{cm} need to be low and by taking the advantages of high output resistance and low voltage operation of current mirror, the $A_v \approx 1$ can be obtained. Another promising design of unity gain voltage buffer is the proposed transconductance enhanced bulk driven OTA with current shunt auxiliary differential pairs as demonstrated in [40]. As shown in Figure 14, M_5 and M6 are diode-connected while M_7 and M_8 act as current sinks to shunt partial bias current to the ground. By implementing this design, it causes dc and ac currents of auxiliary differential pair experience different paths where only dc current with almost no ac current flow through M_7 and M_8. The impedance at node A is increased due to these separated paths that significantly improves the voltage gain of the auxiliary differential pair close to unity.

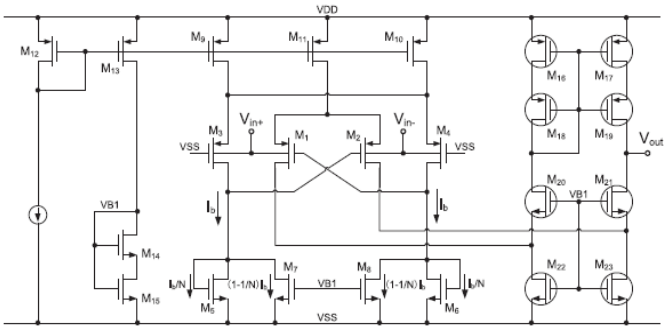

Fig. 14. Transconductance enhanced bulk driven OTA with current shunt auxiliary differential pair [40].

B. Low voltage supply

By designing less complex circuit which can be operated with a voltage supply less than or equal to 1.5 V becomes

one of essential features for low voltage supply or low power portable electronics devices. Novel source-degeneration transconductor, which is based on high performance unity gain voltage buffer was reported in [41].

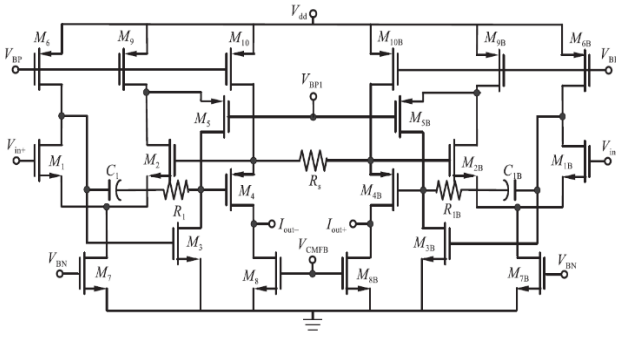

Fig. 15. Source-degeneration transconductor [41].

As shown in Figure 15, the transconductor composes of two identical sub circuits, M_1-M_{10} and M_{1B}-M_{10B}. These two identical sub circuits represent two unity gain buffers. Transistors, M_3 and M_5 acting as a current source will reduce the minimum voltage supply to $V_T + 3_{VDSsat}$ as indicator to a low voltage supply.

The driving point output resistance is reduced to:

$$r_0 \cong \frac{1}{g_{m4}g_{m3}([g_{m5}r_{05}(r_{09}||\, r_{09})]||r_{03})g_{m1}(r_{01}||r_{06})} \quad (4)$$

since the loop gain is boosted by the folded cascode stage. The linearity of the buffer is improved through this small output resistance which result a high linearity transconductor. The resistor, R_s is driven by both unity gain buffers to transfer the input voltage to the transconductor resistor.

[42] demonstrates a new low voltage source degenerated transconductor as shown in Figure 16.

Nearly similar to the previous design where it consists a pair of unity gain buffers which are connected by R. The output resistance of source node is kept very low with a very high output resistance of the drain node.

In addition, by making M_2 works in a weak inversion and keep saturated, the product of $r_{02}g_{m2}$ can be high enough even can reach up to GΩ. Through this equation,

$$r_{out} \approx r_{01}r_{02}g_{m2}(r_{04}||r_{03})g_{m3} \approx r_{01}r_{02}g_{m2}r_{03}g_{m3} \quad (5)$$

the value of output resistance, r_{out} will increase. It will cause the value of V_{GS2} reduces and V_{DS2} can be operated in a low voltage operation. Thus, through weak inversion region, the regulated cascode sources of the transconductor may operate in a low voltage and suitable for low power devices.

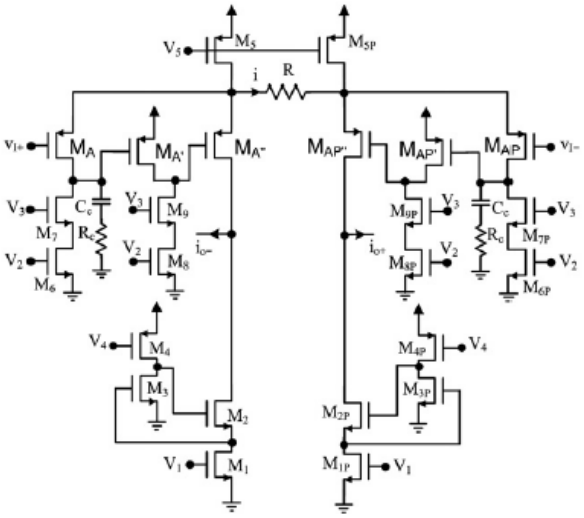

Fig. 16. Low voltage source degenerated transconductor [42].

A FVF based current mirror (CM) using dynamic threshold biasing (DTMOS) technique is demonstrated in [43]. CM as one of most versatile active analog block is usually used in performing analog signal processing. Its essential features are relatively high output resistance and relatively low input resistance. Thus, regardless of load condition, it will keep a constant input and output. Ideally, CM is simply a current amplifier with a gain of -1. Through body effect, the value of V_{th} can be reduced and it enables a variety of effective body biasing technique.

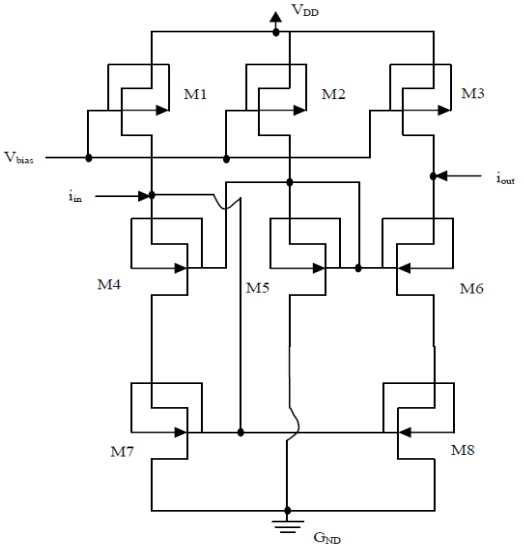

Fig. 17. FVF based current mirror using DTMOS technique [43].

Figure 17 presents FVF based CM using DTMOS technique where the body of each transistors, M_1-M_3 and M_4-M_8 are connected to gate electrode using DTMOS technique. Due to this, when gate input increases, the source-body junction gets slightly forward biased and therefore resulting a reduction in V_{th}. Indirectly, it means through body effect, the FVF based CM can be operated with a low power supply.

The proposed low power class AB version of the FVF in [17] is demonstrated as in Figure 18. M_5 is a dc level shifter and high impedance input node Y is provided by two identical current sources formed by M_1 and M_7. A low voltage cascode CM is formed by M_6, M_7 and M_8 where the transistors duplicate the current through M_2 to M_7. Due to this, CM can be operated with a minimum operating voltage, $V_T + V_{Dsat}$ which is halved of the conventional cascode CM.

In addition, the FVF is modified to be able to maintain the output node at a constant voltage with respect to the input and minimizing the biasing current, I_B i.e FVF is able to sink and source relatively large currents for low voltage and low power consumption.

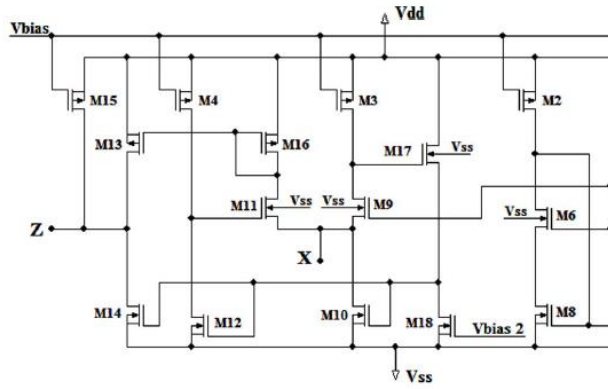

Fig. 18. Low power FVF based Class AB [17].

C. High linearity

A voltage buffer is operating in a linear region if its output signal strength varies proportional to the input signal strength i.e. the output-versus input signal amplitude characteristics appears as a straight line. Then, the slope of the line will determine its gain. The steeper the slope the greater the gain, linearity is better. However, if the input signal is too strong, then the voltage buffer will be working in non-linear region and this will lead to signal distortion. Therefore, the purpose of having a negative feedback loop is to improve the linearity of the voltage buffer.

However, the value of the gain will limit several other voltage buffer performances such as low slew rate, reduce bandwidth, increases power consumption and also stability. Thus, the enhanced source-degeneration CMOS differential transconductor which has been discussed earlier is also capable of improving the linearity problems occurred in voltage buffer [42].

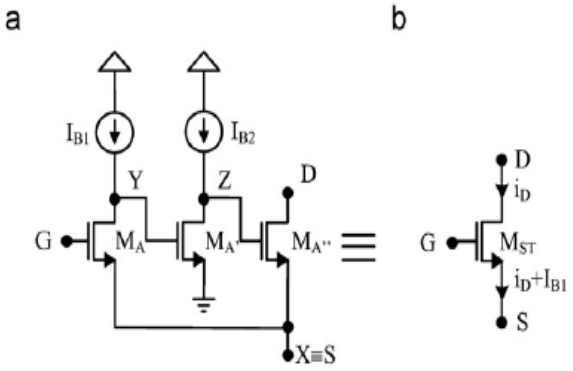

Fig.19. (a) Super transistor and (b) symbol [42].

Basically, the construction of enhanced source-degeneration CMOS differential transconductor is based on super transistor as shown in Figure 19 [42] in improving the operational transconductance amplifier. The advantages of super transistor are unity voltage gain, low output resistance of the source node and very high output resistance of the drain node which later enhances the linearity of voltage buffer.

As mentioned before, by keeping M_2 works in a weak inversion and high value of $r_{02}g_{m2}$ and r_{out} will optimize the transconductor to be operated in low voltage, reduce power consumption but still with high linearity.

[16] demonstrates a highly linear voltage follower which is based on combination of FVF with a negative feedback loop and a cascode transistor with dynamic biasing. M_3 as the cascode transistor and also V_{AB} as floating battery are used in enhancing the linearity of FVF as shown in Figure 20.

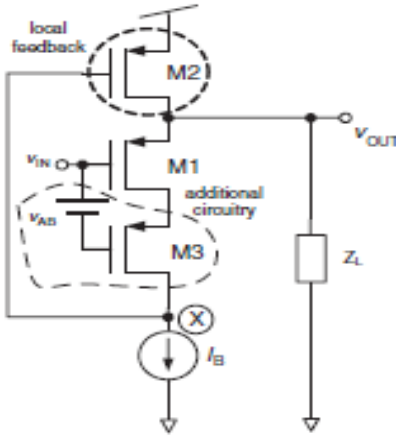

Fig. 20. Highly linear FVF [16].

From the figure, V_{GS}, V_{DS} and V_{BS} will determine I_{DS}. Thus, if I_{DS}, V_{DS} and V_{BS} are kept constant in M_1, V_{GS} would be necessary constant regardless of V_{IN}. In order to force V_{DS} to a constant value, the value of V_{BS} of M1 must be made 0, the current through M1 must be made to constant value through feedback loop and V_{GS} is also need to be constant. This can only be done by adding M_3 and V_{AB}. Therefore, this kind of arrangement will allow the voltage buffer operates in high linearity with the same quiescent power consumption compare to the original FVF.

Another proposed design is source follower based switched capacitor (SC) amplifier for improving linearity but with low power consumption [44]. Figure 21 presents a source follower which based on pseudodifferential input pairs where M3 and M4 duplicate the input signal of M1 and M2. M1 and M2 work as source followers and their bulks are connected to their sources. The input signals of M3 and M4 are replicated to the drains of M1 and M2 as the input transistors. M1-M4 are made to work in saturation region by increasing the values of $V_{in}+$ and $V_{in}-$ larger than $V_{th1,2} + V_{OV3,4} + V_{OV1,2} + V_{OV,\,bias}$. It will then suppress the channel length modulation effect and eliminating bulk effect. With a given bias current, the V_{gs} of the following transistor is nearly constant. Thus, high linearity is achieved and this kind of source follower is suitable to be used in pipelined ADCs.

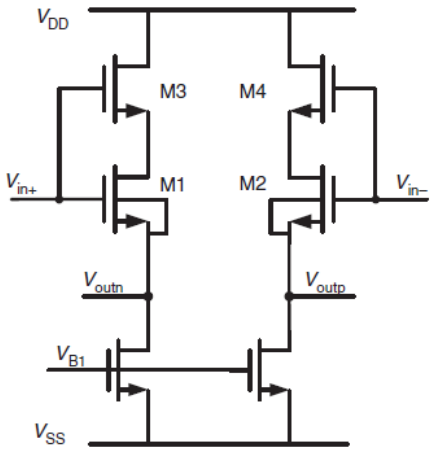

Fig. 21. Source follower for pipelined ADCs [44].

D. Low total harmonic distortion

[45] states that high linearity of voltage buffer will reduce total harmonic distortion (THD). However, high linearity will reduce the performance of the transconductance and increase power consumption.

When a circuit is connected to a non-linear load, the output waveform easily get distorted. i.e., alteration of sinusoid shape. THD is defined as the summation of all harmonic components of the output waveform compared to the input waveform. The higher the percentage, the higher the distortion, the higher the temperature and the higher power consumption.

Figure 22 in [45] presents a new configuration of operational transconductance amplifier. It consists of a differential input source degeneration as input stage and four CM at the output stage i.e. combination techniques of source degeneration and FVF. Through p-type current mirrors M7-M10, the input stage currents are differentially mirrored and the n-type current mirrors, M3-M6 are mirrored to the outputs. In the triode region is M16 and M17. Through M11-M15, the gate voltages of M16 and M17 are connected to I_{bias}. For a large value of transconductance, the channel length is designed as minimum as possible. The triode transistor are connected either in parallel or series depending on respective purposes either for power consumption or high tuning respectively. In this design, by varying the bias voltage (V_B), it will then control the transconductance value. V_B is controlled by I_{bias} through M11-M15. Thus, to reduce THD, the linearity is set to be higher by controlling V_B which then set high value of transconductance.

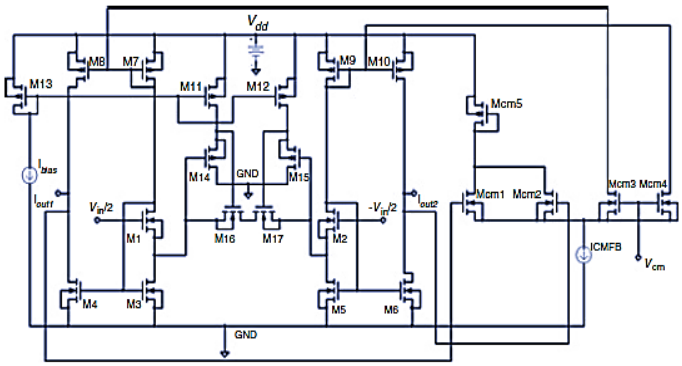

Fig. 22. Operational transconductance amplifier [45].

A fully differential CMOS transconductor based on FVF in combination with mobility reduction compensation is presented to reduce THD in [28].

In mobility reduction compensation, two voltage-to-current converters with the same sign of the fundamental harmonic and opposite signs for the 3rd order harmonic are used to reduce nonlinearity aspect where the transistors will be working in saturated and weak inversion region as shown in Figure 23.

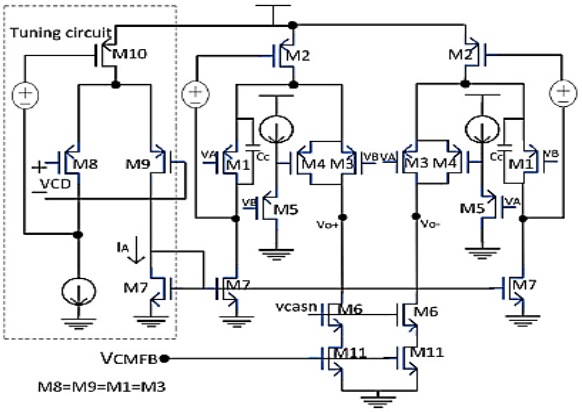

Fig. 23. CMOS fully differential linear transconductor [28].

Further, to increase the input range, stability and output impedance, $R_{out} \sim r_{03}$, a level shifter, a compensation capacitor C_r and cascode transistor M_6 are added respectively. During operation, weak inversion transistor (M_4) is in parallel with main input transistor (M_3) which is working in saturated region. By increasing the width of M_4 by M5, THD which is initially dominated by H_3 will decrease. When a minimum of THD is reached, it will be then dominated by H_5. So, the output current of the transconductor is the combination of currents from M3 and M4. Thus, linearity can be improved by selecting a proper ratio of M_4 and M_5.

Recent improvement of source follower buffer has been reported in [46]. Figure 24 shows the source follower buffer where through this design, the third harmonic (H3) is directly neutralized without being influenced by its source.

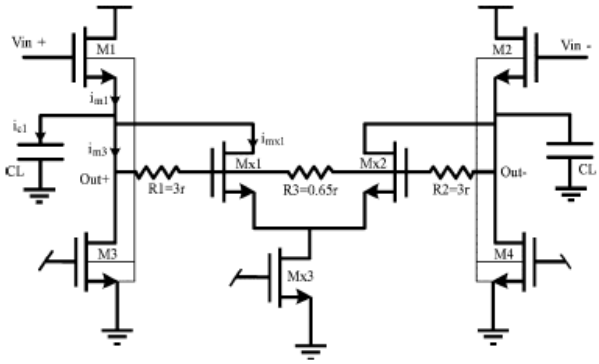

Fig. 24. Source follower buffer [46].

This linearization technique improves linearity by neutralizing H3 without sacrificing bandwidth and power consumption. An extra part is added (at the middle between the two source buffer) so that H3 component of the transistor's current is absorbed to ensure only small fraction of H3 left in load capacitor's current. It means, H3 is degraded by setting H3 main driver transistor to be same with H3 of neutralized transistor. A third harmonics absorption circuit is a differential pair with fixed bias current. Thus, through this technique, higher linearity with low THD are achieved by lowering down H3.

E. Wide bandwidth

In designing wireless and high speed devices, wide bandwidth is one of crucial aspect to be considered. A few techniques have been discovered in designing wide bandwidth in analog devices such as resistive compensation [47], capacitive compensation [48], feedforward compensation [49] and inductive peaking [50].

Ref. [51] demonstrates a new FVF with bandwidth enhancement by using inductive peaking technique. Through this technique, by adding inductive element (Z) in the negative feedback loop of FVF will increase the impedance path and reduce the current flow. Z is shown in Figure 25 in between M1 and M2.

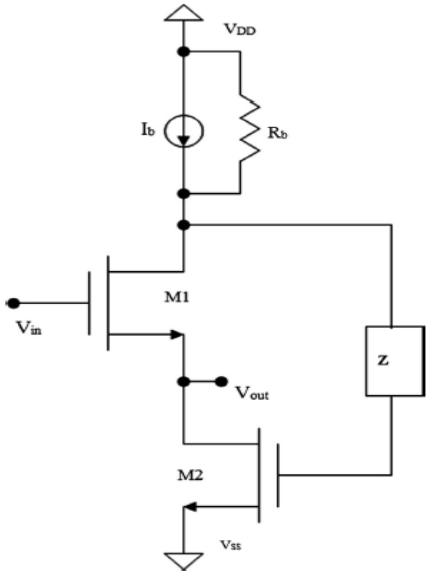

Fig. 25. Flipped voltage follower with bandwidth enhancement [51].

The current will be forced to flow to output path which has a lower impedance i.e. the current in the feedback path is delayed. This will cause more current in the output node, the charging time in capacitor is reduced and thereby the bandwidth is increased without any additional power dissipation.

Another design of voltage buffer for bandwidth enhancement is reported in [29] which is based on

combination of differential FVF (DFVF) with current comparison technique. As being shown in Figure 26, the current comparator circuit (b) is added to ensure M3 is provided with low current when it is connected to any load.

The voltage of M3 has to be controlled in order to avoid M3 sinks with large current. Thus, in this combination, the size of M3 will modify the resistance of the discharging path so that it may reduce the difference between the rise and fall time. By increasing the values of R_c and C_c to make both tune to obtain same rise and fall times responses, it will then reduce THD. In addition, through simulation, [29] has reported that the bandwidth is improved from 2.4 MHz by using DFVF without current comparator to 6.2 MHz. Another design of FVF in enhancing bandwidth has been discussed earlier in Figure 5. By using typical FVF topology with additional transistor acting as an adaptable current source, this design may achieve class AB behavior. Through experimental analysis, it shows that the bandwidth is near 200MHz for C_L=1pF.

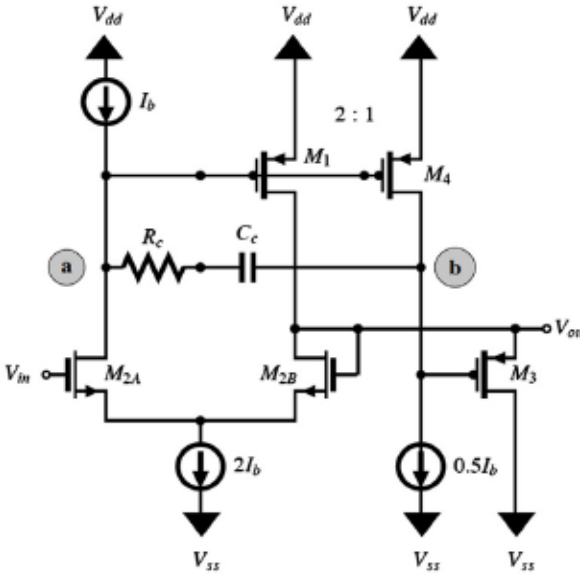

Fig. 26. Differential flipped voltage follower with current comparator [29].

F. High slew rate

Slew rate can be defined as the maximum rate of change of output voltage per unit of time. It is expressed as volts per second. In designing a buffer with a high gain in i.e. closely to unity, the slew rate will decrease. In addition, when the input to a buffer is too high with a large amplitude, it will also decrease slew rate. Thus, in driving a large capacitor loads such as a switched capacitor circuits, it is important to ensure the buffer has a high slew rate and a small or fast settling time [14].

[14] demonstrates a buffer amplifier which consist of two complementary differential inputs with a common source push pull output stage, M_N/ M_P as shown in Figure 27.

The output PMOS transistor, M_P for sourcing current is driven by an NMOS input stage and M_{1a}-M_{5a}. Meanwhile, for sinking current, the output NMOS transistor, M_N is driven by a PMOS input stage M_{1b}-M_{5b}. The slew rate enhancement circuits are $M_{6a/b}$-$M_{8a/b}$ where rising slew rate enhancement will be by M_{6a}-M_{8a} and falling slew enhancement by M_{6b}-M_{8b}.

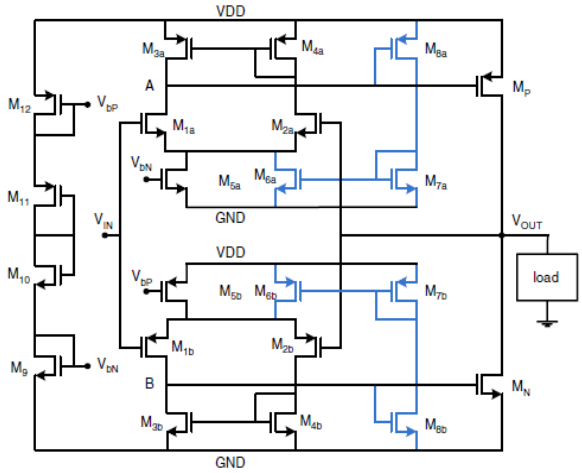

Fig. 27. Buffer amplifier [14].

During slewing, when V_{IN} experiences a large low-to high step signals, the current will flow to M_{3a} from M_{5a} causes decreasing in V_a and turning on M_{8a}. M_{6a}-M_{8a} will then provide additional current to the upper part input pair. Thus, more dynamic current is provided which then improve the slew rate of the buffer.

Another design for slew rate enhancement amplifier is discussed in [52] with a combination of a buffer amplifier with a biasing circuit. Figure 28 shows the two pairs M19, M20 and M31, M32 acting as the fall and rise slew sensors.

At a sufficient large rising step input at V_{IP} where the circuit enters the slewing state, the tail current, I_{N2} flows through M20, then it is copied by M24 and M28 will saturate. M29 will turn on due to drain voltage of M28 where the tail current for M1 and M2 is added to enhance the slew rate. A similar mechanism for a falling step input signal where the tail current for M3 and M4 is added by M31 and M32. Thus, by having these slew rate sensors, the slew rate is improved throughout the entire rail to rail signal range.

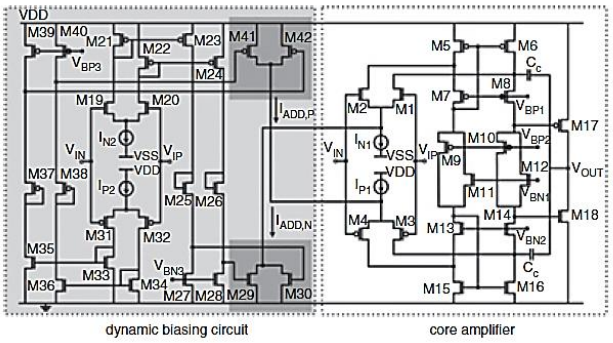

Fig. 28. Buffer amplifier [52].

As being discussed earlier in [24], super class AB BD OTA is based on bulk flipped voltage follower for the bulk driven input stage and a nonlinear current mirror in order to improve the slew rate of flipped voltage follower.

From the figure, M2(*N*), M3(*N*) and M4(*N*) act as nonlinear current mirror to improve the slew rate. M2(*N*) will be in saturation region when the current through it is $I_B + I_{MB}$ under quiescent condition. In slewing condition, M2(*N*) is injected with high current generated by the input stage and forcing it into triode region. Thus, the output current is changed and will enhance the slew rate.

A summary of CMOS voltage buffer performances as discussed before is shown in Table 2.

Countless architectures are proposed to improve the performance of CMOS voltage buffer in order to make it as closely as possible or approximately as an ideal voltage buffer. Besides able to duplicate the output signal as the same as its input, ideal voltage buffer should also be able to sense the input signal without loading the signal source in any way. With the downscaling of CMOS technology, some external factors such as cost efficiency and smaller feature size will grow more and more attention in designing the architecture besides improving its parameters. It becomes really a challenging task to the designers to have all the advantages with minimal limitations in only one architecture.

In this brief, none of the architectures able to improve all the parameters to be regarded as the perfect high performance CMOS voltage buffer. Every new architecture is designed to improve one or a few parameters of the other architecture. As example, [19] improves slew rate which nearly close to [14] but is operated in low voltage supply. The purpose of [45] is to improve total harmonic distortion while [41] and [42] besides suitable for low voltage application, they also improve linearity and total harmonic distortion.

[12] reports that the most essential parameters in designing voltage buffer are unity gain and low output impedance. g_m which denotes as transconductance with body effect are inversely related to this output impedance. Logically, by increasing the value of body effect, the value of output impedance can be reduced. However, this will then reduce the voltage gain. In addition, if large value of g_m is designed for driving large capacitive load by increasing the value of drain current I_D, it will cause serious loading effect, larger value of W/L ratio, increase the size of transistors, high power consumption, reduce voltage swing and bandwidth [12], [21], [41]-[42].

By comparing between [41] and [42], [41] has lower total harmonic distortion but due to its larger value of g_m, its power consumption is greater. It is also similar to [45] where the value of g_m is too large, its power consumption and voltage supply are also higher. However, through the implementation of mobility reduction compensation technique, [28] can be operated with a very low voltage supply, low power consumption, low total harmonic distortion and high linearity even the value of g_m is higher in [28] than in [41] and [42].

Linearity of the voltage buffer is strongly influenced by g_m and total harmonic distortion [41], [42], [45], [46]. By measuring the total harmonic distortion, its linearity can be determined. The higher the total harmonic distortion, the higher the output signal is being distorted and this will cause more current, higher temperature, higher power dissipation and higher power consumption [45]. Besides that body effect, channel length modulations, signal dependent capacitive efforts and frequency dependent distortion are several common non-ideal effects that create trade-off between linearity, bandwidth and power consumption in designing voltage buffer [35]. In this modern world, it is often required to produce total harmonic distortion less than -80 db [41] and usually, TVF and OTA will be the chosen architectures to achieve low total harmonic distortion with high linearity [45]. Further, by comparing [44] and [46], both designs improve linearity of the voltage buffer but produce high power consumption. It is reported in [46], through linearization technique, the power consumption is increased 14% for every 10 dB linearity compared to the conventional buffer. In addition, [13] reports that high linearity will also relatively lead to stability problem, poor bandwidth and low slew rate.

However, by introducing a feedback loop as in FVF, it may improve linearity [16], widen the bandwidth [17], [34], [51] and improve slew rate i.e. high slew rate [9], [14]. Indeed, it will then increase the complexity of the circuit.

Table 2. CMOS voltage buffer performances.

Year published [Ref. no]	Topology	CMOS process (µm)	Voltage supply (V)	THD (dB)	Power (mW)	Input swing (Vp-p)	Bandwidth (MHz)	Gm (µS)	Slew rate +/- (V/µs)	Settling time +/- (µs)
1999 [11]	VF with current mirror and enhancement-mode MOS transistors	0.18	2.5	-	0.3562	1.5	-	-	-	-
2015 [40]	BD OTA	0.18	0.5	-	0.026	-	0.00326	-	840/590	640
2009 [41]	TVF	0.18	1.2	-80 @ 1MHz	0.240	0.4	-	50	-	-
2011 [42]	TVF	0.13	1.5	-110 @ 11 kHz	0.126	0.35	50	40	-	-
2013 [43]	FVF with current mirror	0.25	1.2	-	0.102	-	168.48	-	-	-
2013 [17]	Class AB FVF	0.35	1.15	-	0.195	-	57.2	-	-	-
2011 [16]	FVF with cascode transistor and floating battery	0.5	1.2	-99 @ 1 MHz -68 @ 5 MHz	-	1.0	-	-	-	-
2015 [44]	VF based switched capacitor amplifier	0.065	1.2	-65.9 @ 122.3 MHz	1.44	1.0	-	-	-	0.002
2008 [45]	TVF	0.18	1.8	-40 @ 1MHz	11.8	0.85	-	1100	-	-
2012 [28]	FVF with mobility reduction compensation technique	0.13	1.0	-55 @ 5MHz	0.045	0.4	-	88	-	-
2015 [46]	VF with linearization technique	0.35	1.5	-86 @100 MHz -95 @ 100 MHz	48	1.6 1.0	-	-	-	-
2013 [51]	FVF with inductive peaking technique	0.18	1.5	-	0.006	-	5461	-	-	-
2013 [29]	DFVF with current comparator	0.5	3.0	-55 @ 100 kHz	0.225	0.3	6.2	-	3.5/ 4.3	-
2015 [19]	Bulk driven class AB FVF	0.35	1.2	-	0.03	-	200	-	29/ 27.7	-
2010 [14]	VF with slew rate enhancement technique	0.18 0.35	3.3 12	-	-	-	-	-	18/18.5 25/23	0.45/0.4 1.4/1.5
2012 [52]	VF with dynamic biasing circuit	0.35	3.3	-	-	-	-	-	2.75	-
2015 [24]	BD OTA	0.18	1.0	-	-	0.8	2.9	-	3.95	0.42

It can be seen that [39], [19] and [43] which are based on the implementation of voltage follower with shunt feedback, the voltage buffers are operated with wide bandwidths. Due to high demand in wireless devices, voltage buffer with wide bandwidth will offer wider useful frequency range but it tends to dissipate high power [39]. However, in [14] where the voltage buffer is designed without any feedback loop still can produce high slew rate through the slew rate enhancement technique based on the adaptive current biasing scheme. Without any feedback loop, [14] occupies smaller layout area and smaller number of transistors.

In further discussing on slew rate, in driving a large capacitive or resistive load, it is important to design voltage buffer with high slew rate and high voltage swing in order to ensure the output signal does not take such a long time to rise and fall [13]-[14]. Fast settling time in voltage buffer leads to high slew rate where a low slew rate may introduce error in its output signal. In addition, low voltage swing may lead to low linearity which will affect the performance of voltage buffer. However, voltage buffer which offers high slew rate and high voltage swing will use large power consumption and lead to complexity [53]. Another interesting point is if the buffer is designed with high gain in which closely to unity gain, the slew rate is decreased. In addition, when the input to a buffer is too high with a large amplitude, it will then limit the slew rate at the output.

In order to ensure the gate oxide reliability and to fulfill the consumer electronics market, in designing voltage buffer, it is essential for the device to be operated in a low voltage [1], approximately equal or below 1.5V. However, if the input voltage is lowered than the threshold voltage, it will create effect to the linearity of the voltage buffer [12]. In order to reduce this problem, one of the suggested ways is by applying a bias voltage to the body or substrate terminal of the transistor, so that the threshold voltage can be modulated electronically and even reduced by the body effect [43]. However, as discussed above, body effect may lower down by the voltage supply [43] but it may distort the voltage gain and degrade the performance of voltage buffer [11].

V. CONCLUSION

This review article has discussed several various common topologies and architectures of voltage buffer and several crucial parameters that contribute to a high performance voltage buffer. From this review, we conclude that the selection of the voltage buffer topology plays important roles in determining the complexity of the problem to be solved, its requirements and the purpose of its application. Each topology has its own advantages and limitations. In addition, each parameter and any combination therefore shows great influence to each other and ultimately decides the performance. We surmise this work will help the designers in this field for designing or selecting a suitable architecture by keeping in minds about all the limitations and challenges discussed throughout for better optimization based on its pertinent parameters such voltage-gain, linearity, total harmonic distortion, bandwidth, slew rate, power consumption, speed, driving capability, voltage swing, noise performance and power efficiency.

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